

***Compal Confidential***

***PBL01***

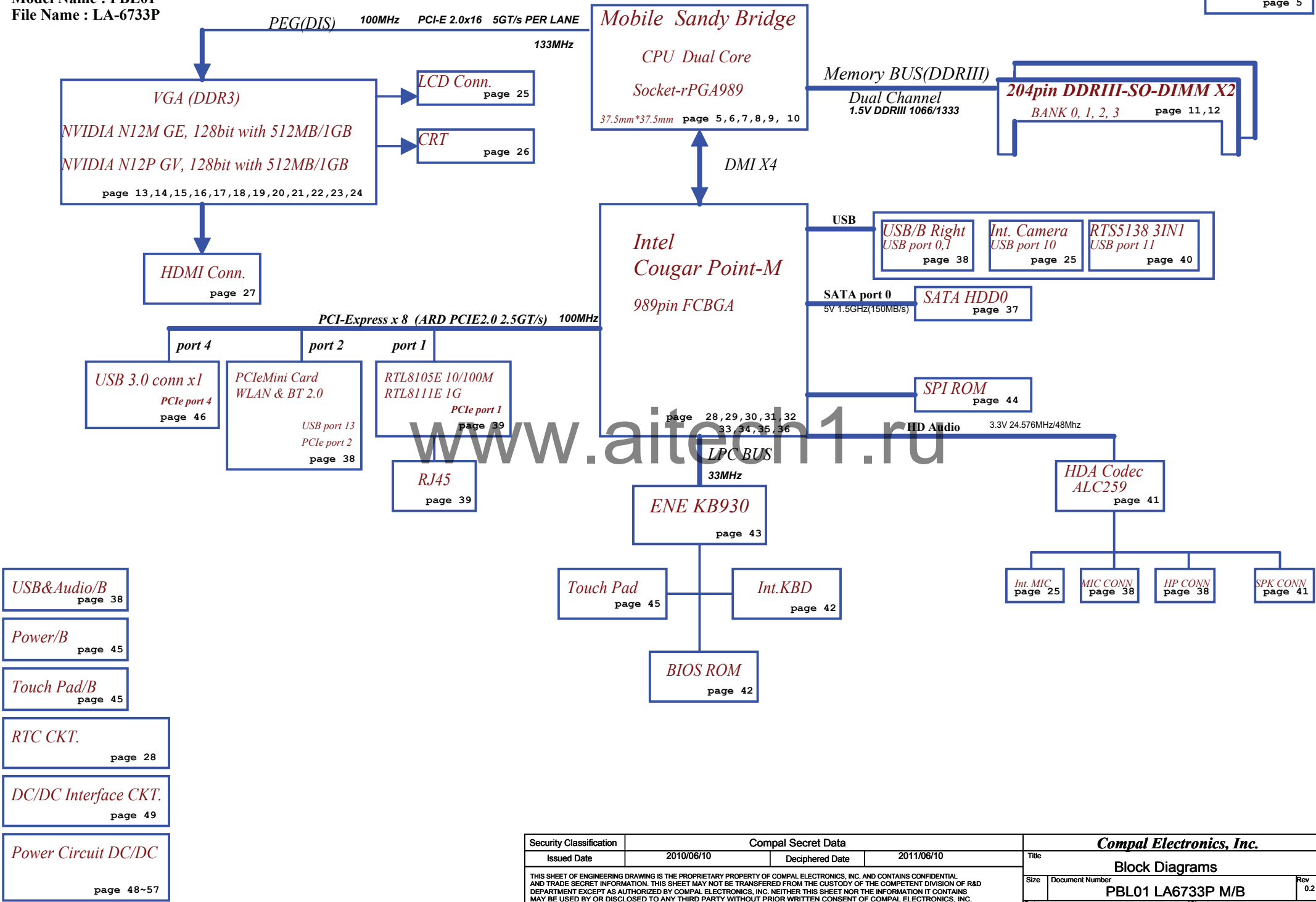
**LA-6733P REV 0.3 Schematic**

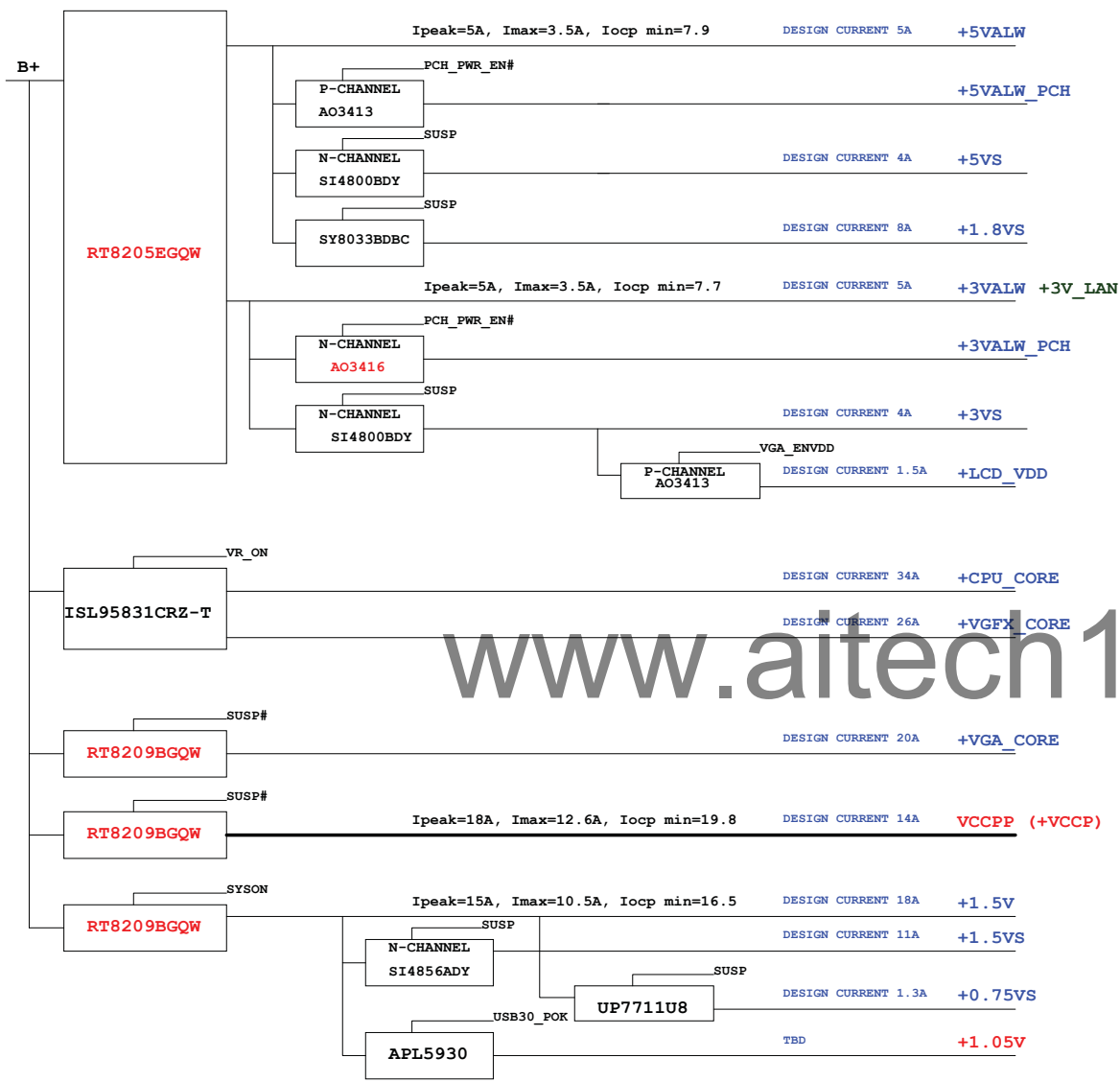
Intel Sandy Bridge/Cougar Point

DIS

2010-11-02 Rev. 0.3

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+VCCP	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

Power	Device	Address
+3VALW	EC KB930	
+3VL	Smart Battery	0001 011x b

EC SM Bus2 address

Power	Device	Address
+3VS	EC KB930	
+3VS	GPU Thermal Sensor	
+3VALW	PCH	

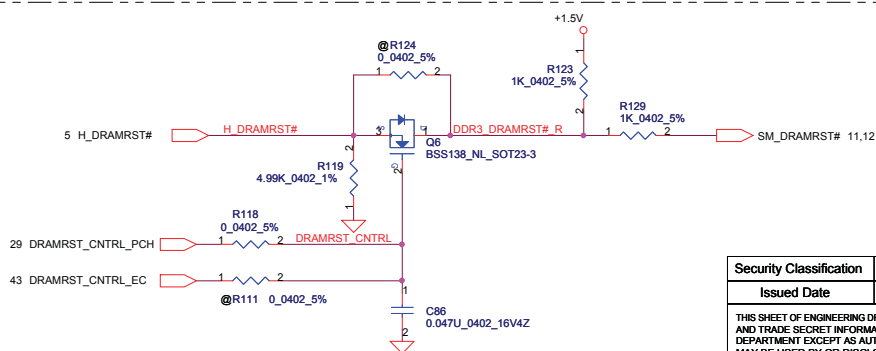
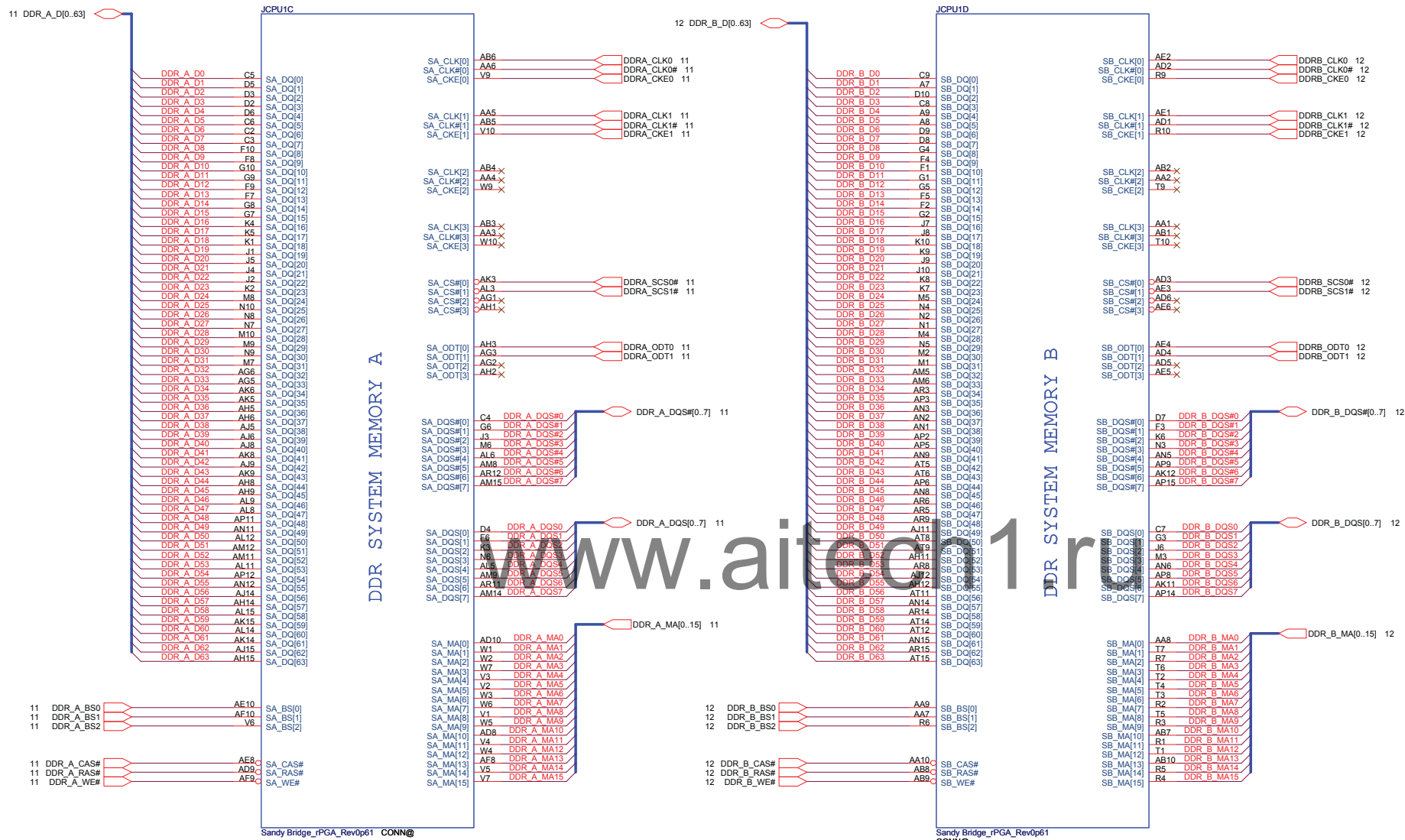
PCH SM Bus address

Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMMA	1001 000x b
+3VS	DDR DIMMB	1001 010x b
+3VS	Slot#1-WLAN	

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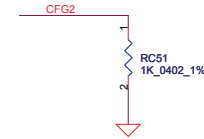
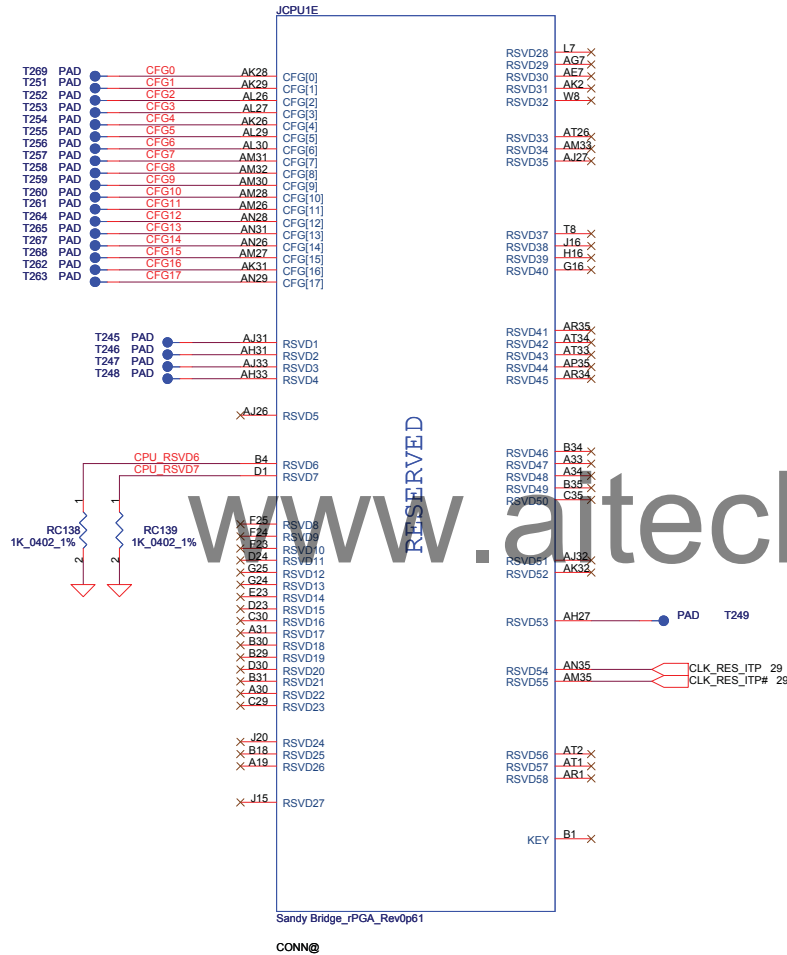




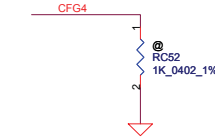
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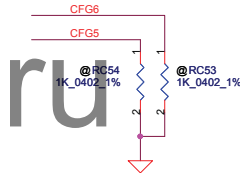
## CFG Straps for Processor



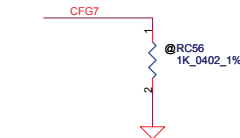
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



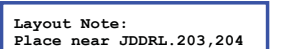
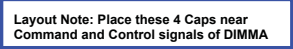
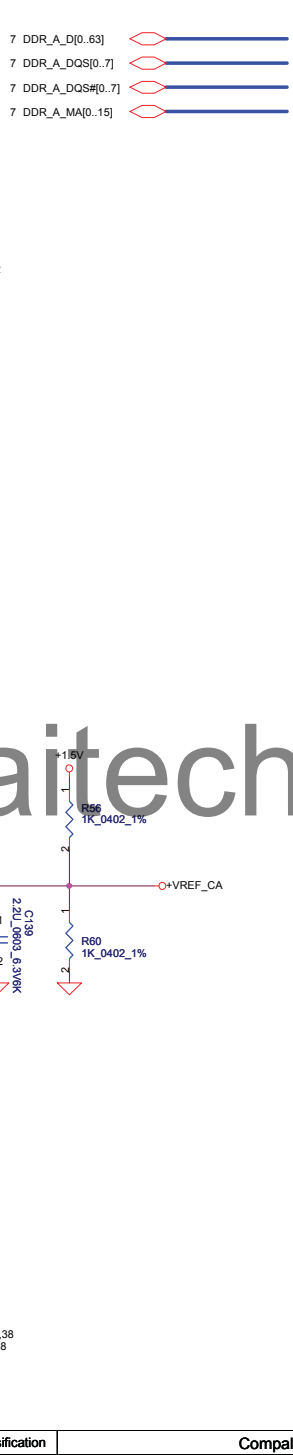
PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



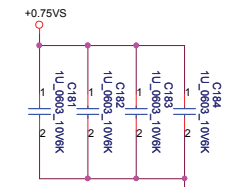
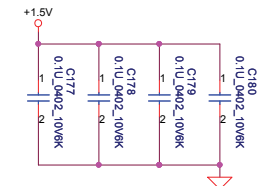
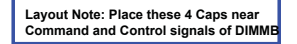
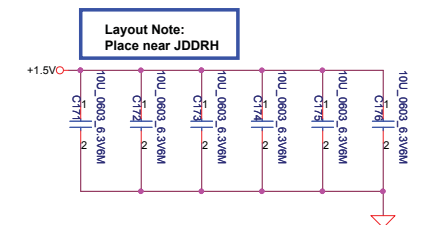
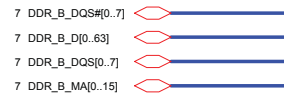
PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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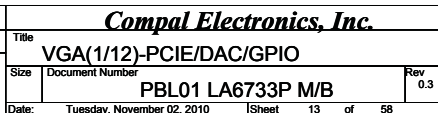


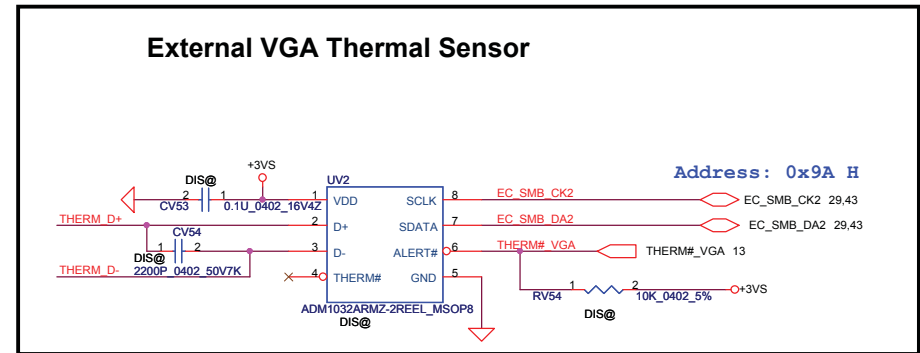
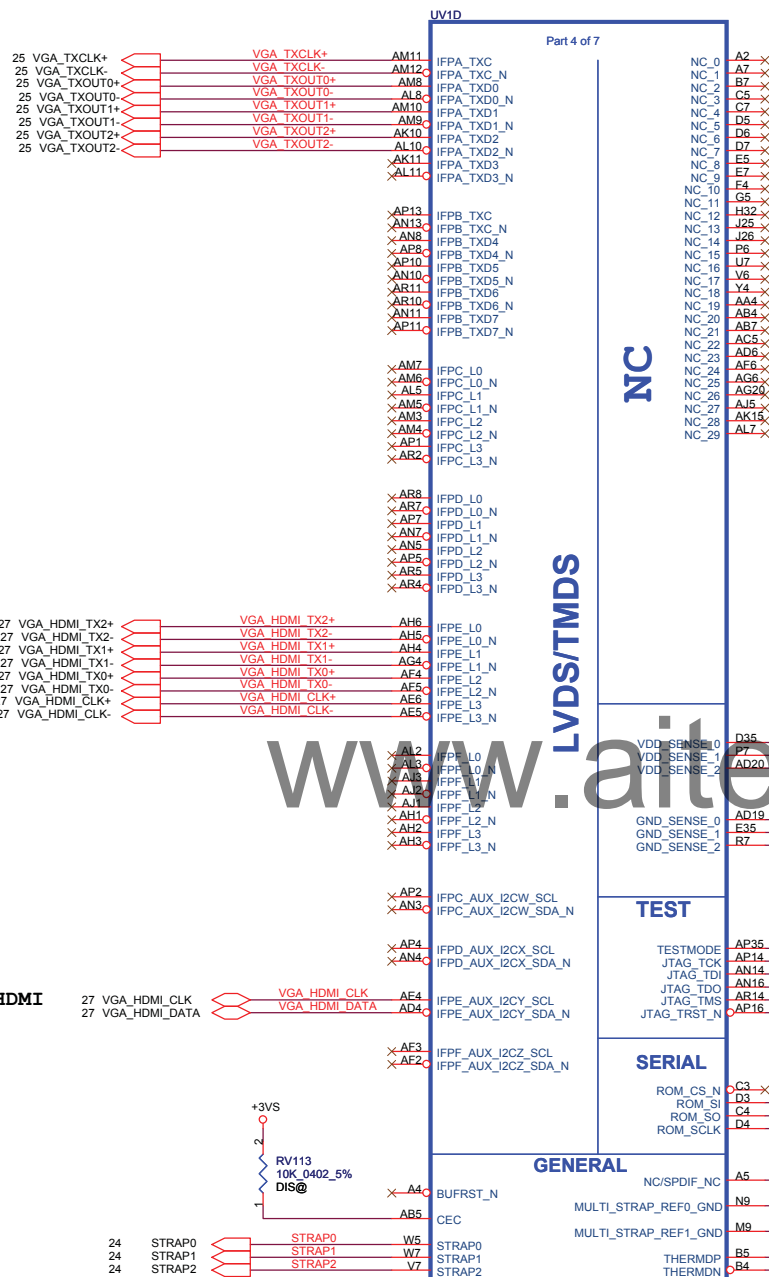
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DDR6\_CLK1 7  
DDR6\_CLK1# 7  
DDR\_B\_BS1 7  
DDR\_B\_RAS# 7  
DDR6\_SC0# 7

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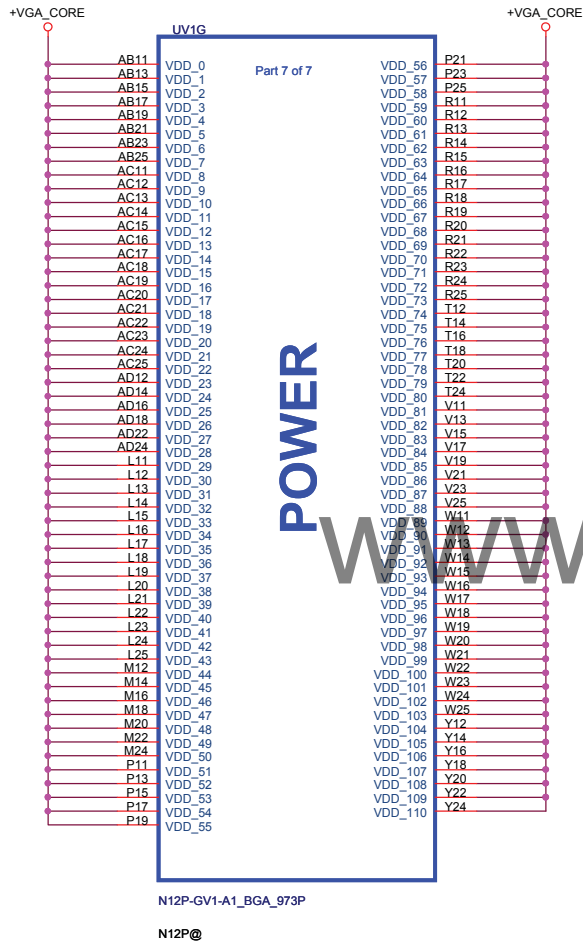
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# N12M-GE-B Performance Mode

Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0			1.0 V
P8-P12			0.85 V

# N12P-GV1 Performance Mode

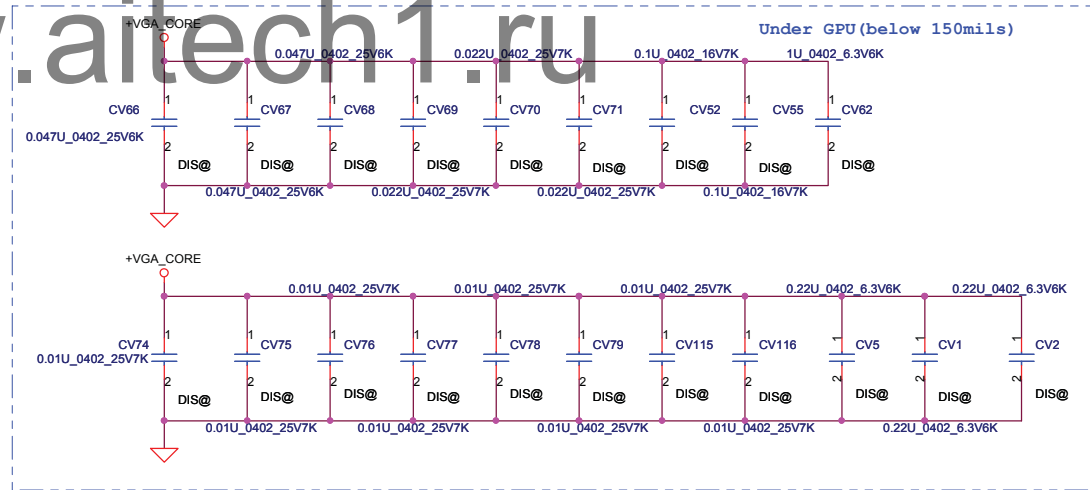
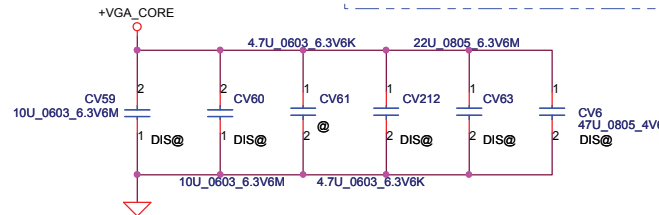
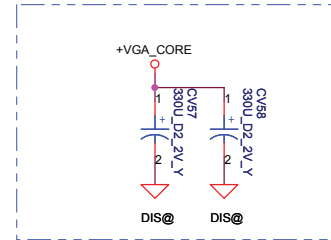
Mode	NVCLK (MHz)	MCLK (MHz)	+VGA_CORE
P0 (Cold)			0.925 V
P0 (Hot)			0.875 V
P8-P12			0.825 V



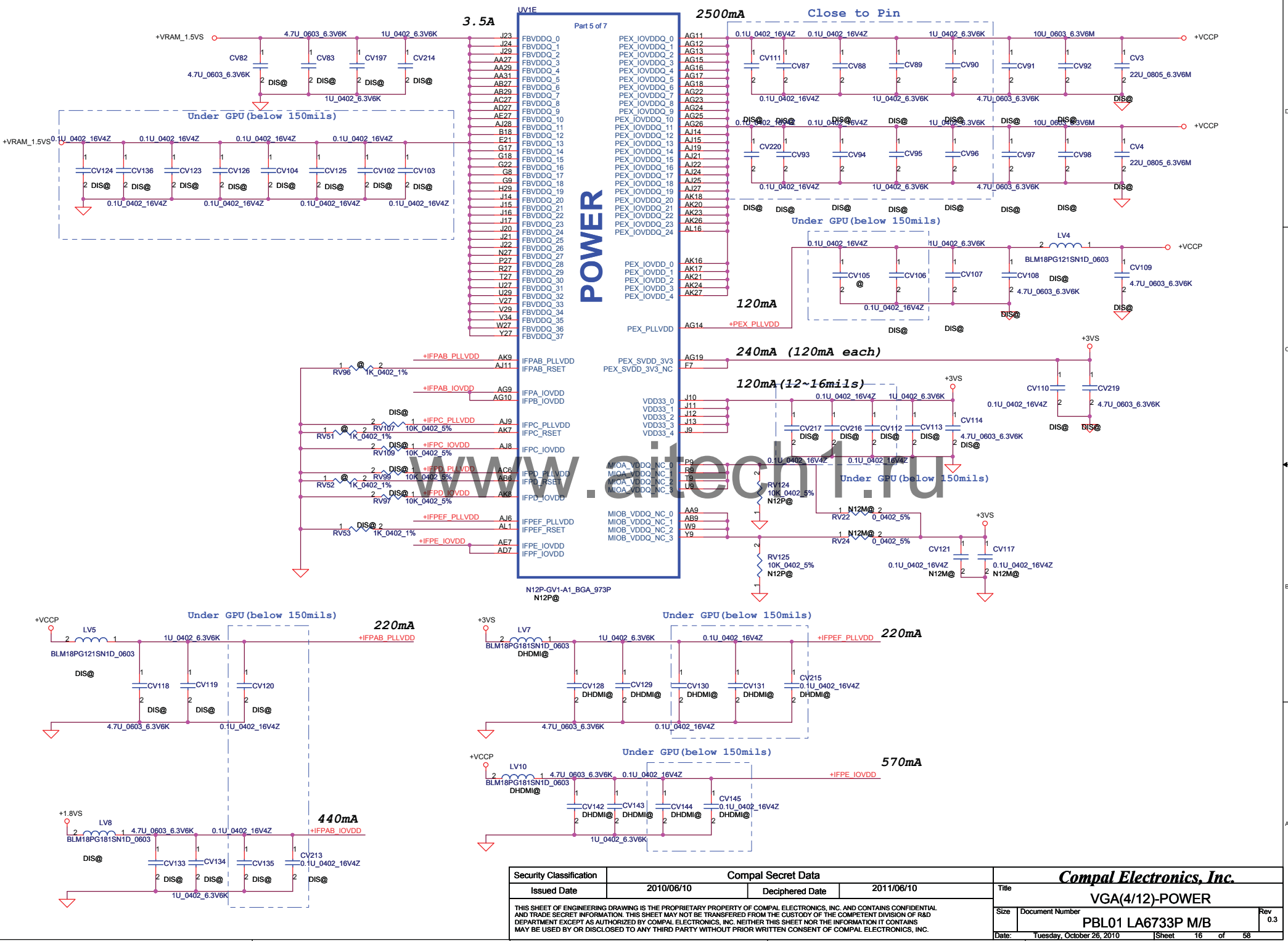
N12P-GV1-A1\_BGA\_973P

N12P@

Near to PL901



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N12P-GV1-A1\_BGA\_973P  
N12P@

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UV1B

Part 2 of 7

MDA0	L32	FBA_D0
MDA1	N33	FBA_D1
MDA2	L33	FBA_D2
MDA3	N34	FBA_D3
MDA4	P35	FBA_D4
MDA5	P35	FBA_D5
MDA6	P33	FBA_D6
MDA7	P34	FBA_D7
MDA8	K35	FBA_D8
MDA9	K33	FBA_D9
MDA10	K34	FBA_D10
MDA11	H33	FBA_D11
MDA12	G34	FBA_D12
MDA13	G33	FBA_D13
MDA14	E34	FBA_D14
MDA15	E33	FBA_D15
MDA16	G31	FBA_D16
MDA17	F30	FBA_D17
MDA18	G30	FBA_D18
MDA19	G32	FBA_D19
MDA20	K30	FBA_D20
MDA21	K32	FBA_D21
MDA22	H30	FBA_D22
MDA23	K31	FBA_D23
MDA24	L31	FBA_D24
MDA25	L30	FBA_D25
MDA26	M32	FBA_D26
MDA27	N30	FBA_D27
MDA28	M30	FBA_D28
MDA29	F31	FBA_D29
MDA30	R32	FBA_D30
MDA31	R30	FBA_D31
MDA32	AG30	FBA_D32
MDA33	AG32	FBA_D33
MDA34	AH31	FBA_D34
MDA35	AF31	FBA_D35
MDA36	AF30	FBA_D36
MDA37	AE30	FBA_D37
MDA38	AC32	FBA_D38
MDA39	AD30	FBA_D39
MDA40	AN33	FBA_D40
MDA41	AL31	FBA_D41
MDA42	AM33	FBA_D42
MDA43	AL35	FBA_D43
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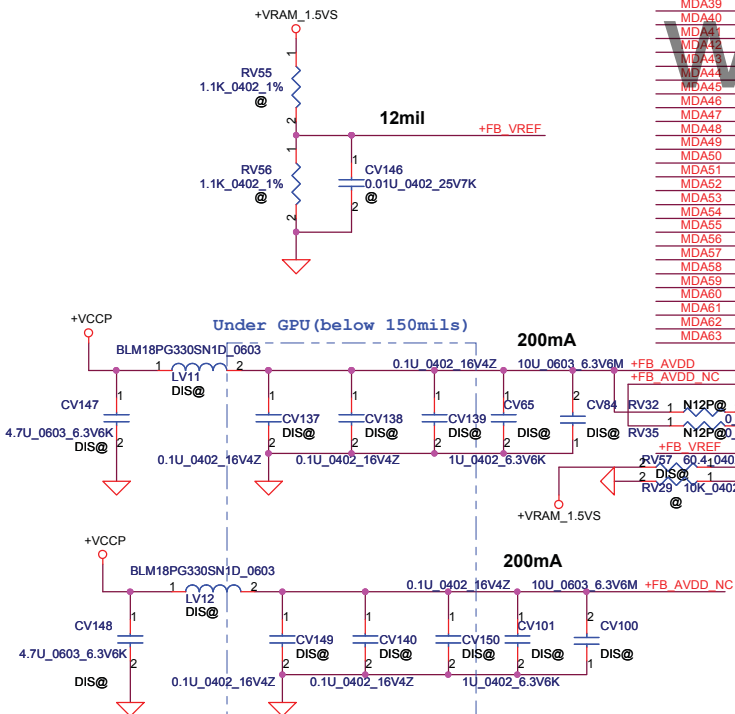
MEMORY INTERFACE

FBA_CMD0	U30	CMDA0	CMDA0	20
FBA_CMD1	V30	CMDA2	CMDA2	20
FBA_CMD2	U31	CMDA3	CMDA3	20
FBA_CMD3	V32	CMDA4	CMDA4	20,21
FBA_CMD4	T35	CMDA5	CMDA5	20,21
FBA_CMD5	W32	CMDA6	CMDA6	20,21
FBA_CMD6	W33	CMDA7	CMDA7	20,21
FBA_CMD7	W31	CMDA8	CMDA8	20,21
FBA_CMD8	W34	CMDA9	CMDA9	20,21
FBA_CMD9	U34	CMDA10	CMDA10	20,21
FBA_CMD10	U35	CMDA11	CMDA11	20,21
FBA_CMD11	U32	CMDA12	CMDA12	20,21
FBA_CMD12	T34	CMDA13	CMDA13	20,21
FBA_CMD13	T33	CMDA14	CMDA14	20,21
FBA_CMD14	W30	CMDA15	CMDA15	20,21
FBA_CMD15	AB30	CMDA16	CMDA16	21
FBA_CMD16	AA30	CMDA18	CMDA18	21
FBA_CMD17	AB31	CMDA19	CMDA19	21
FBA_CMD18	AA32	CMDA20	CMDA20	20,21
FBA_CMD19	AB33	CMDA21	CMDA21	20,21
FBA_CMD20	Y32	CMDA22	CMDA22	20,21
FBA_CMD21	Y33	CMDA23	CMDA23	20,21
FBA_CMD22	AB34	CMDA24	CMDA24	20,21
FBA_CMD23	AB35	CMDA25	CMDA25	20,21
FBA_CMD24	Y35	CMDA26	CMDA26	20,21
FBA_CMD25	W35	CMDA27	CMDA27	20,21
FBA_CMD26	Y34	CMDA28	CMDA28	20,21
FBA_CMD27	Y31	CMDA29	CMDA29	20,21
FBA_CMD28	Y30	CMDA30	CMDA30	20,21
FBA_CMD29	W29	CMDA30	CMDA30	20,21
FBA_CMD30	Y29	CMDA30	CMDA30	20,21
FBA_CMD31	Y29	CMDA30	CMDA30	20,21

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FBA_DQM6	AL34	DQMA6	DQMA[7..0]	20,21
FBA_DQM7	AE35	DQMA7	DQMA[7..0]	20,21
FBA_DQS_RN0	D35	DQSA#0	DQSA[7..0]	20,21
FBA_DQS_RN1	G35	DQSA#1	DQSA[7..0]	20,21
FBA_DQS_RN2	H31	DQSA#2	DQSA[7..0]	20,21
FBA_DQS_RN3	M32	DQSA#3	DQSA[7..0]	20,21
FBA_DQS_RN4	AD32	DQSA#4	DQSA[7..0]	20,21
FBA_DQS_RN5	AJ31	DQSA#5	DQSA[7..0]	20,21
FBA_DQS_RN6	AJ35	DQSA#6	DQSA[7..0]	20,21
FBA_DQS_RN7	AC34	DQSA#7	DQSA[7..0]	20,21
FBA_DQS_WP0	L34	DQSA0	DQSA[7..0]	20,21
FBA_DQS_WP1	H35	DQSA1	DQSA[7..0]	20,21
FBA_DQS_WP2	J32	DQSA2	DQSA[7..0]	20,21
FBA_DQS_WP3	N31	DQSA3	DQSA[7..0]	20,21
FBA_DQS_WP4	AE31	DQSA4	DQSA[7..0]	20,21
FBA_DQS_WP5	AJ32	DQSA5	DQSA[7..0]	20,21
FBA_DQS_WP6	AJ34	DQSA6	DQSA[7..0]	20,21
FBA_DQS_WP7	AC33	DQSA7	DQSA[7..0]	20,21
FBA_WCK0	P29	CLKA0	CLKA0	20
FBA_WCK0_N	R29	CLKA0#	CLKA0#	20
FBA_WCK1	L29	CLKA1	CLKA1	21
FBA_WCK1_N	M29	CLKA1#	CLKA1#	21
FBA_WCK2	AG29	CLKA1#	CLKA1#	21
FBA_WCK2_N	AH29	CLKA1#	CLKA1#	21
FBA_WCK3	AD29	CLKA1#	CLKA1#	21
FBA_WCK3_N	AE29	CLKA1#	CLKA1#	21

## Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2



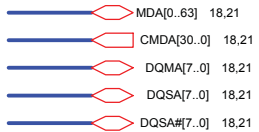
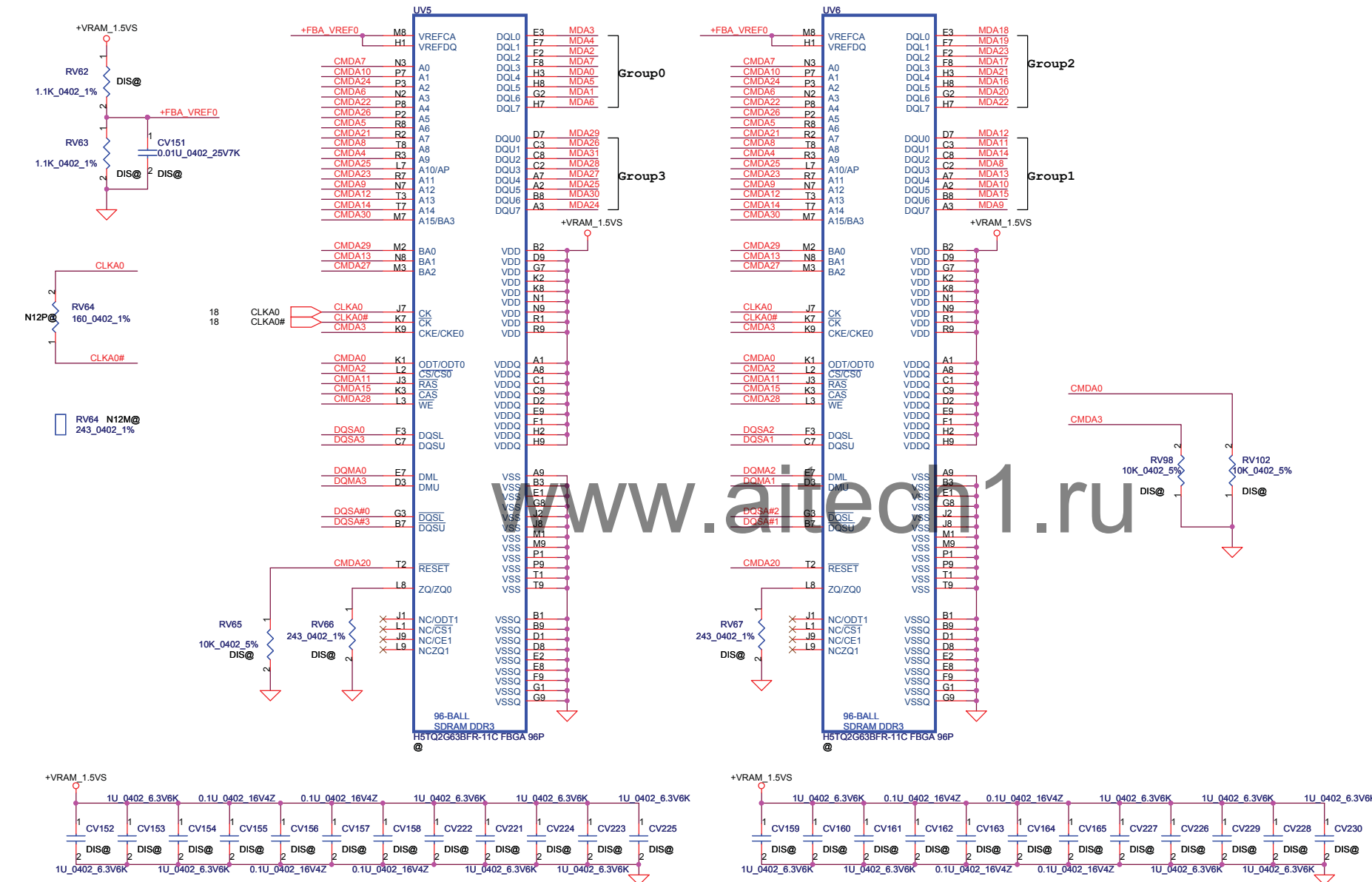
N12P-GV1-A1\_BGA\_973P

N12P@

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				Size	Document Number
				PBL01 LA6733P M/B	
				Date:	Rev
				Tuesday, November 02, 2010	0.3
				Sheet	18 of 58



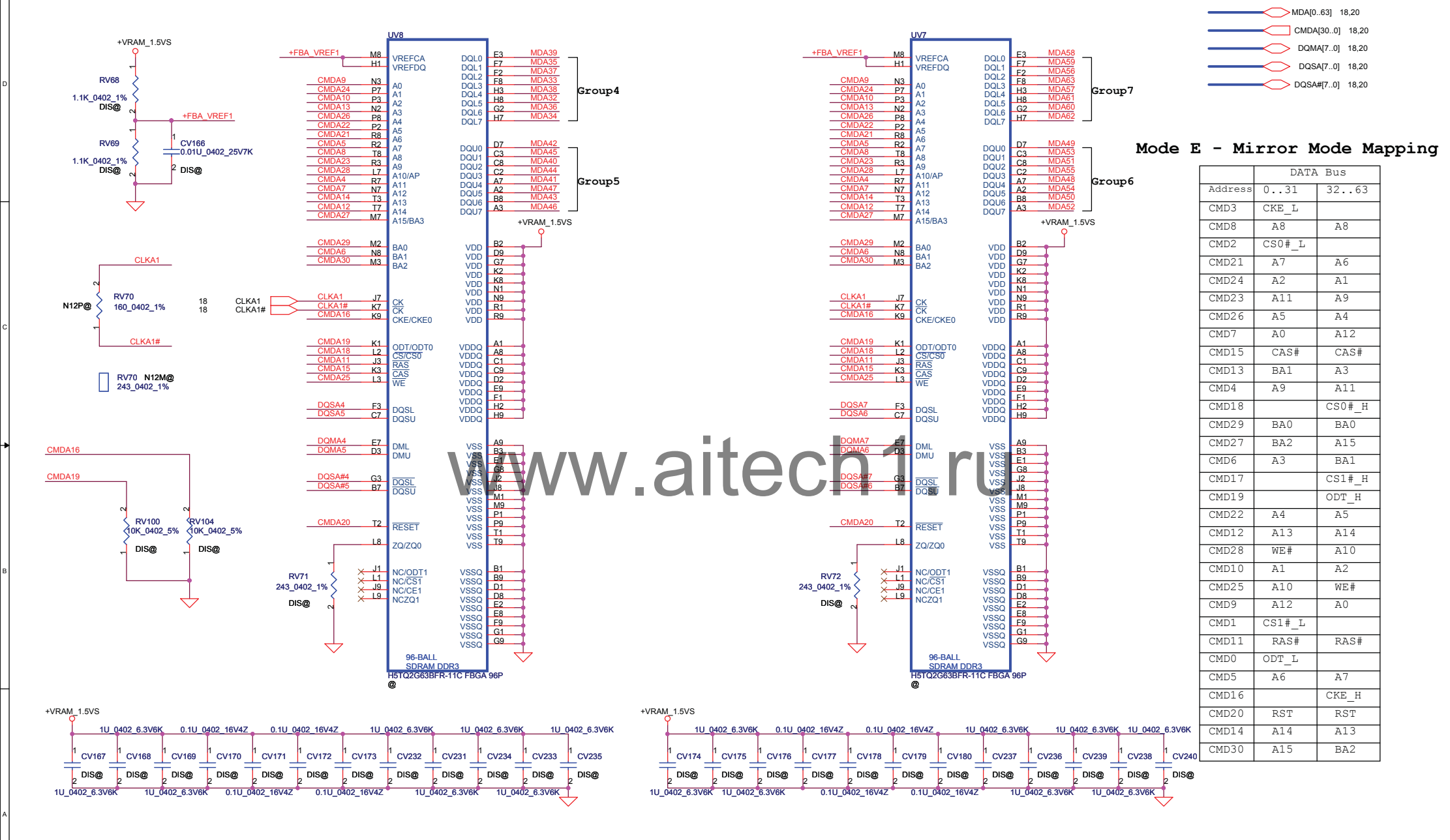
Memory Partition A - Lower 32 bits



Mode E - Mirror Mode Mapping

DATA Bus	
Address	0..31 32..63
CMD8	CKE_L A8
CMD2	CS0#_L A8
CMD21	A7 A6
CMD24	A2 A1
CMD23	A11 A9
CMD26	A5 A4
CMD7	A0 A12
CMD15	CAS# CAS#
CMD13	BA1 A3
CMD4	A9 A11
CMD18	CS0#_H
CMD29	BA0 BA0
CMD27	BA2 A15
CMD6	A3 BA1
CMD17	CS1#_H
CMD19	ODT_H
CMD22	A4 A5
CMD12	A13 A14
CMD28	WE# A10
CMD10	A1 A2
CMD25	A10 WE#
CMD9	A12 A0
CMD1	CS1#_L
CMD11	RAS# RAS#
CMD0	ODT_L
CMD5	A6 A7
CMD16	CKE_H
CMD20	RST RST
CMD14	A14 A13
CMD30	A15 BA2

Memory Partition A - Upper 32 bits

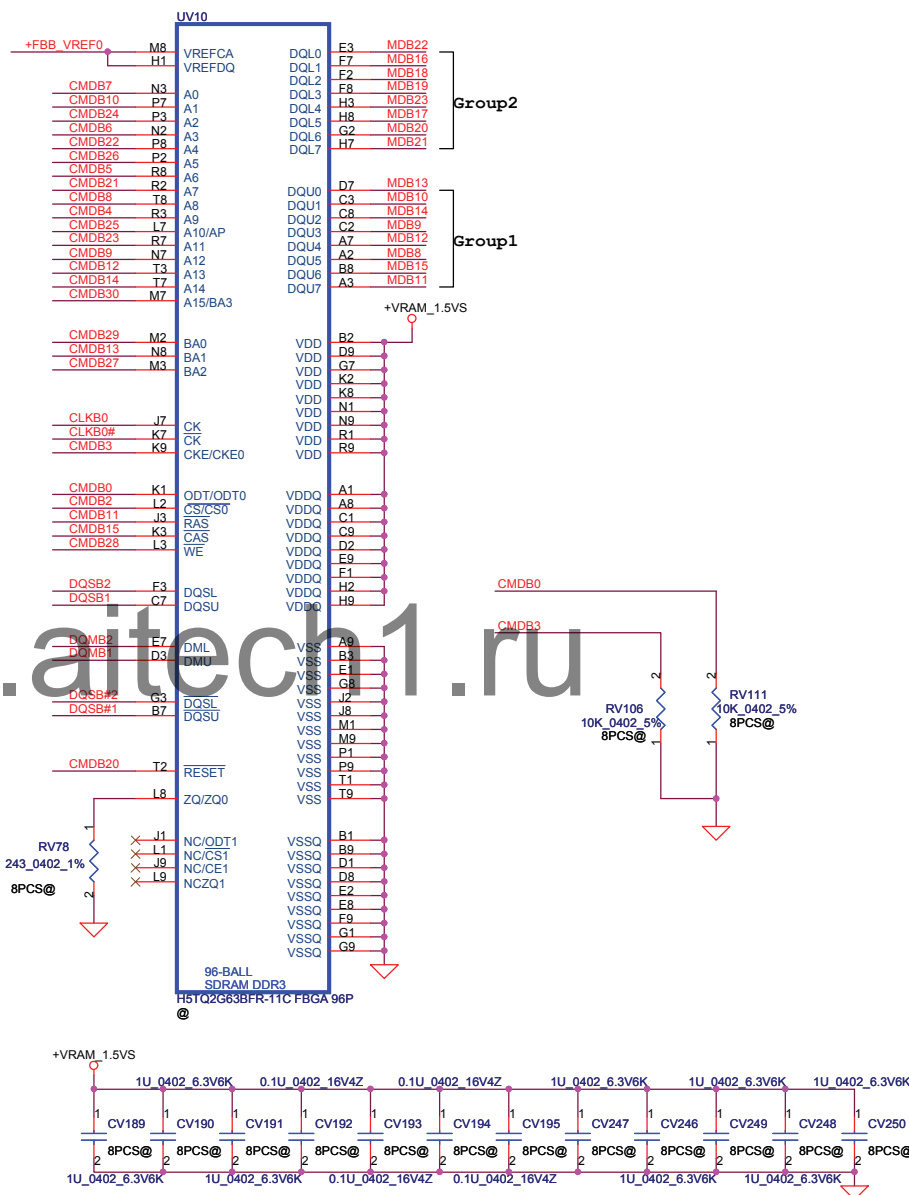


- MDA[0..63] 18,20
- CMDA[30..] 18,20
- DQMA[7..0] 18,20
- DQSA[7..0] 18,20
- DQSA[7..0] 18,20

Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

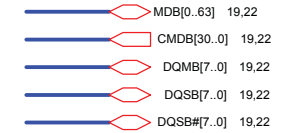
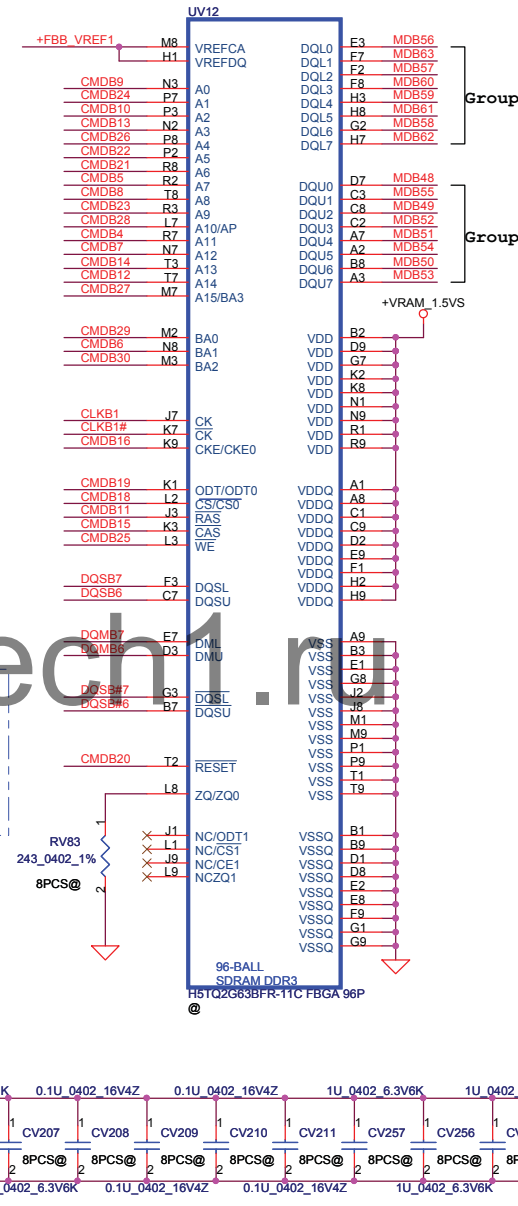
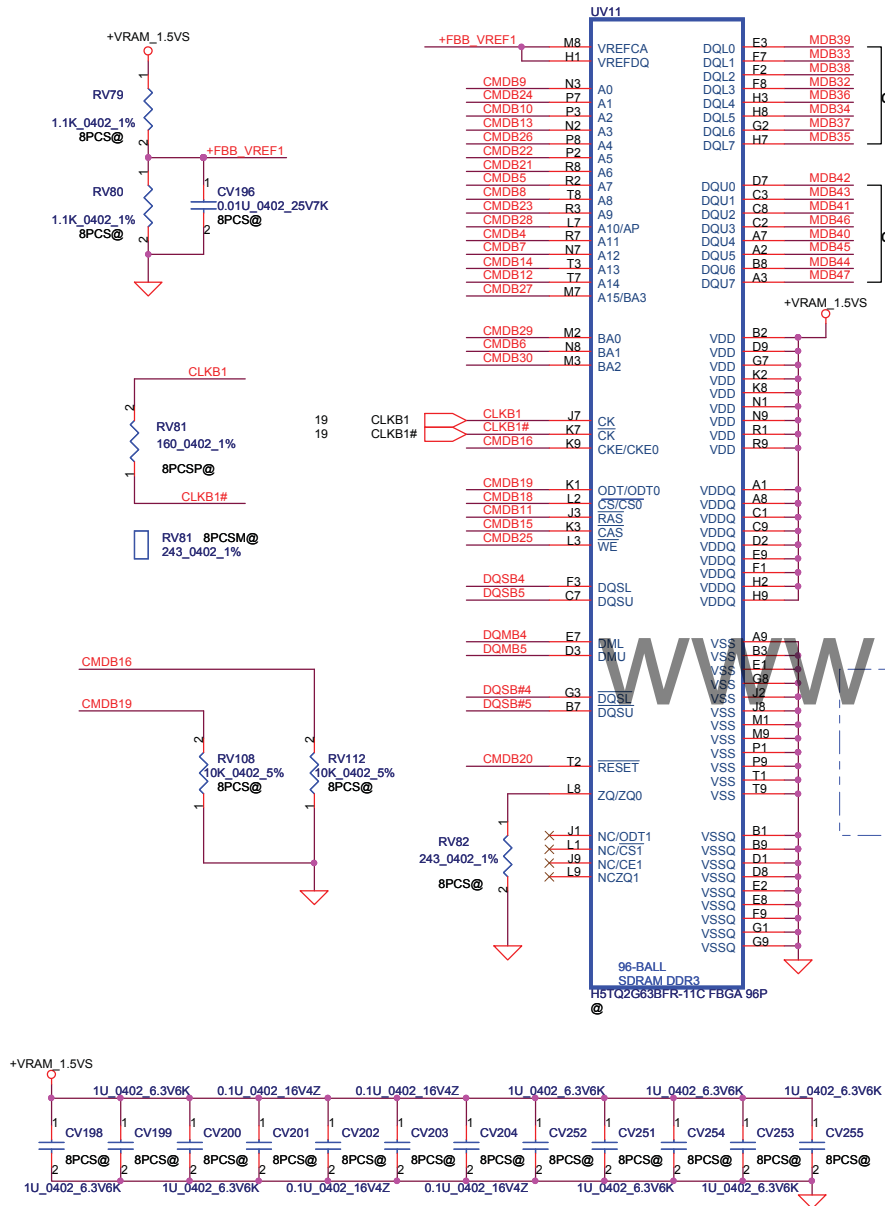
	MDB[0..63]	19,23
	CMDB[30..0]	19,23
	DQMB[7..0]	19,23
	DQSB[7..0]	19,23
	DQSB#[7..0]	19,23



	DATA Bus	
Address	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD28	WE#	A10
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD1	CS1#_L	
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

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# Memory Partition C - Upper 32 bits

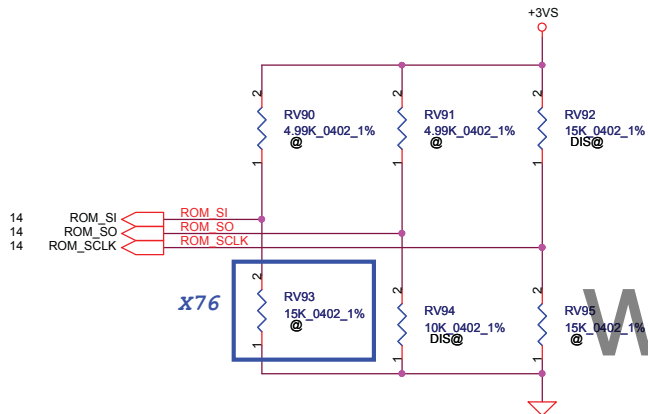
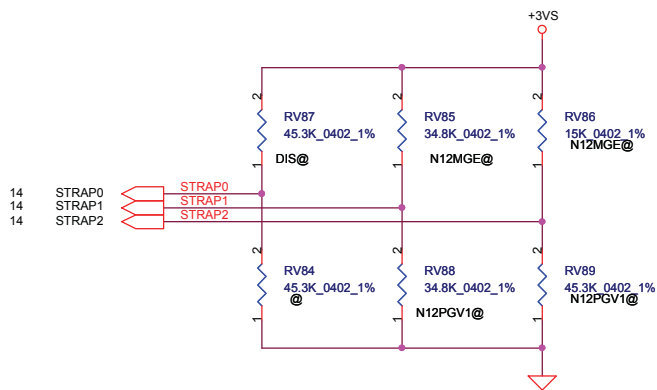


## Mode E - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
CMD3	CKE_L	
CMD8	A8	A8
CMD2	CS0#_L	
CMD21	A7	A6
CMD24	A2	A1
CMD23	A11	A9
CMD26	A5	A4
CMD7	A0	A12
CMD15	CAS#	CAS#
CMD13	BA1	A3
CMD4	A9	A11
CMD18		CS0#_H
CMD29	BA0	BA0
CMD27	BA2	A15
CMD6	A3	BA1
CMD17		CS1#_H
CMD19		ODT_H
CMD22	A4	A5
CMD12	A13	A14
CMD10	A1	A2
CMD25	A10	WE#
CMD9	A12	A0
CMD11	RAS#	RAS#
CMD0	ODT_L	
CMD5	A6	A7
CMD16		CKE_H
CMD20	RST	RST
CMD14	A14	A13
CMD30	A15	BA2

Security Classification		Compal Secret Data		Title	
Issued Date	2010/06/10	Deciphered Date	2011/06/10	VGA(11/12)-VRAM C Upper	
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Rev 0.3



DeviceID	ROM_SCLK	STRAP2
N12M-GE	Pull up 15K	Pull up 15K
N12P-GV1	Pull up 15K	Pull down 45K

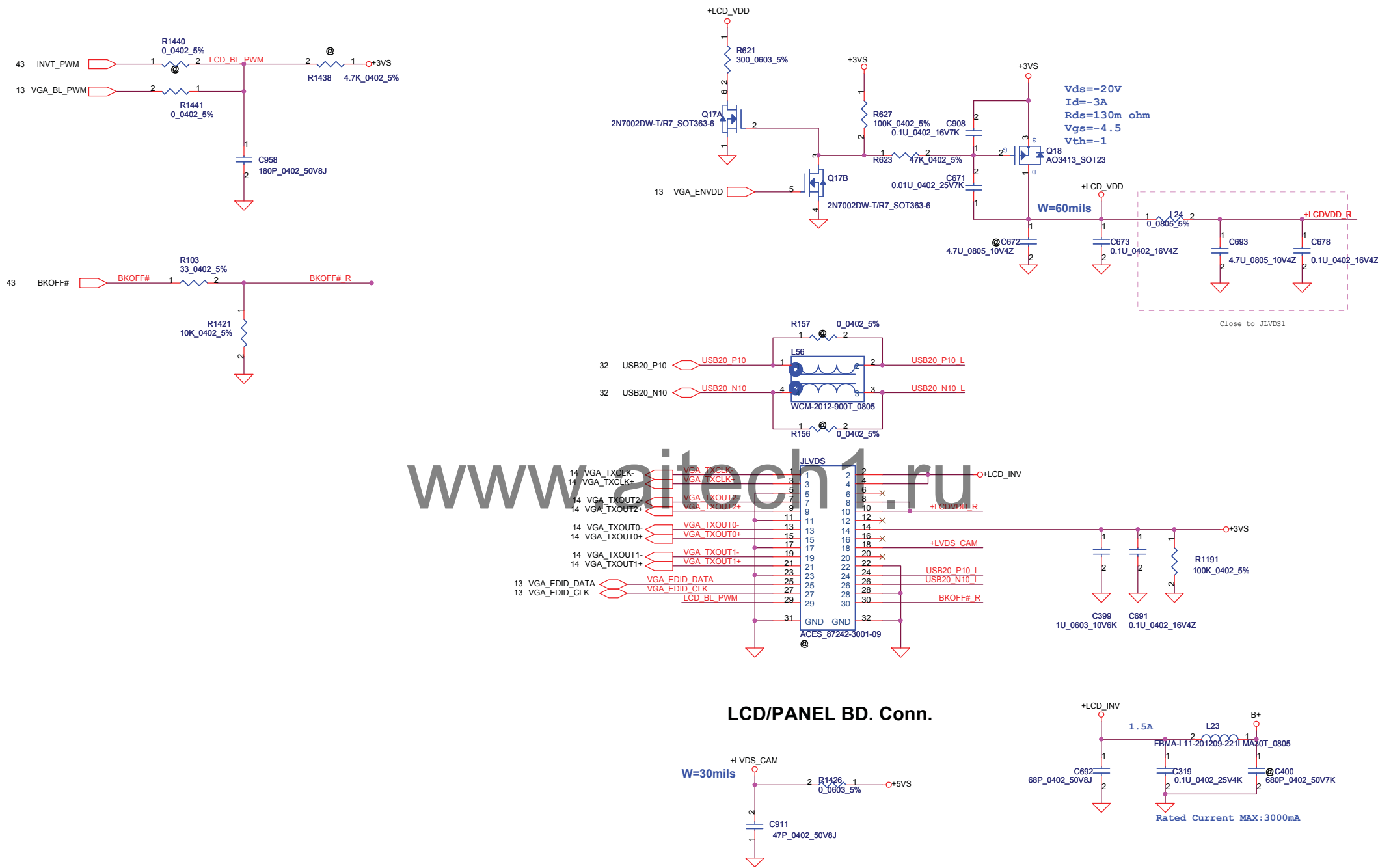
Hynix H5TQ2G63BFR-12C SA00003VS00	1G	0110	PD 34.8K	SD034348280
Samsung K4W2G1646B-HC12 SA00003MQ40	1G	0111	PD 45.3K	SD034453280

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLEN_TERM
ROM_SI	+3VS	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	+3VS	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	+3VS	USER[3]	USER[2]	USER[1]	USER[0]

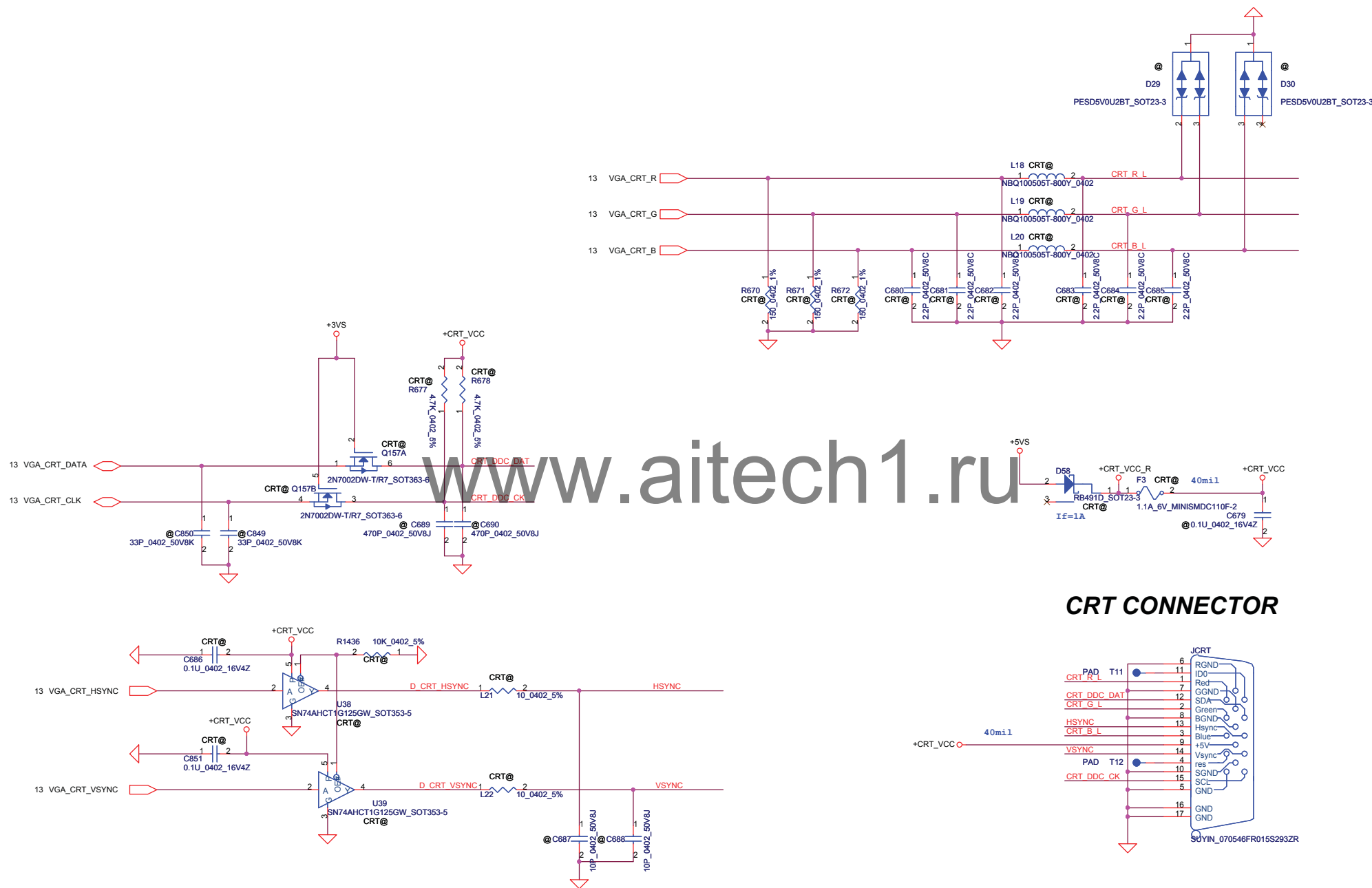
Resistor Values	Pull-up to +3VS	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

<b>SUB_VENDOR</b>		<b>XCLK_417</b>	
0	No VBIOS ROM	0	277MHz (Default)
1	BIOS ROM is present (Default)	1	Reserved
<b>FB_0_BAR_SIZE</b>		<b>USER Straps</b>	
0	256MB (Default)	User[3:0]	
1	Reserved	1000-1100	Customer defined
<b>3GIO_PADCFG</b>		<b>PEX_PLL_EN_TERM</b>	
3GIO_PADCFG[3:0]		0	Disable (Default)
0110	Notebook Default	1	Enable
<b>SLOT_CLK_CFG</b>			
0	GPU and MCH don't share a common reference clock		
1	GPU and MCH share a common reference clock (Default)		
<b>SMBUS_ALT_ADDR</b>		<b>VGA_DEVICE</b>	
0	0x9E (Default)	0	3D Device
1	0x9C (Multi-GPU usage)	1	VGA Device (Default)

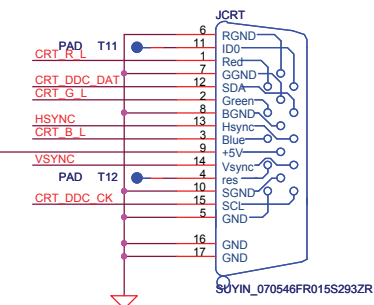
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
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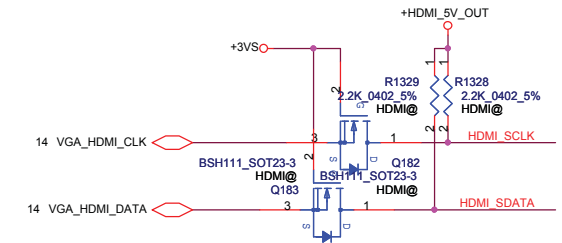
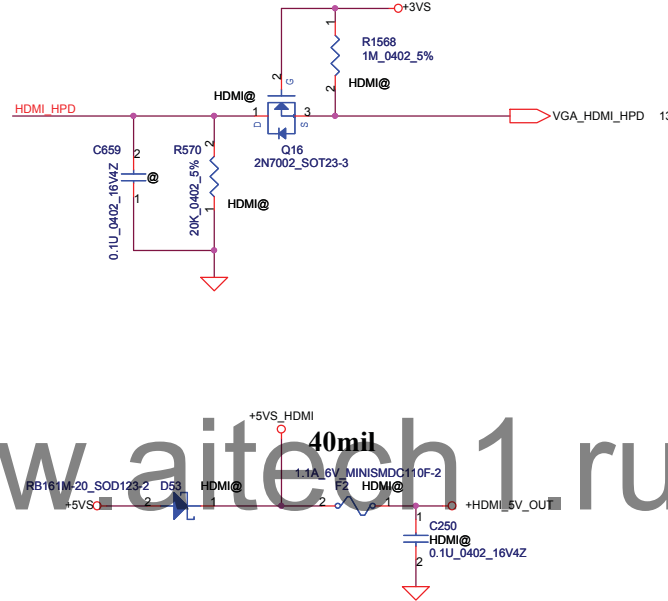
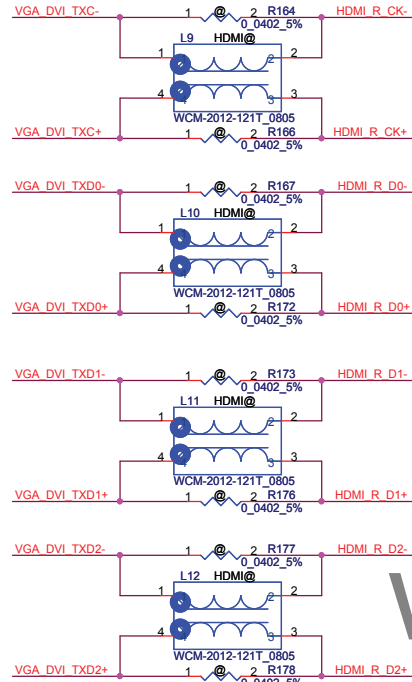
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Issued Date	2010/06/10	Deciphered Date	2011/06/10	Title	
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Size		Document Number		Rev	
		PBL01 LA6733P M/B		0.3	
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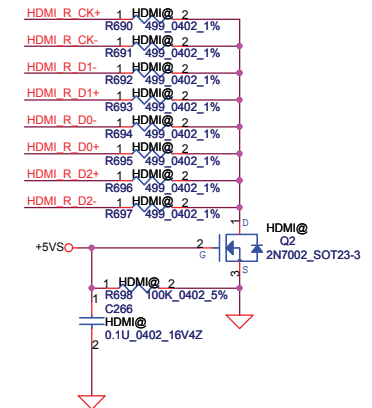
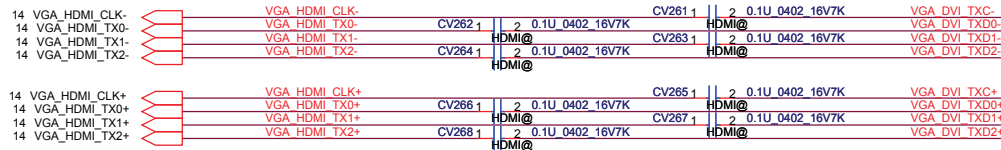
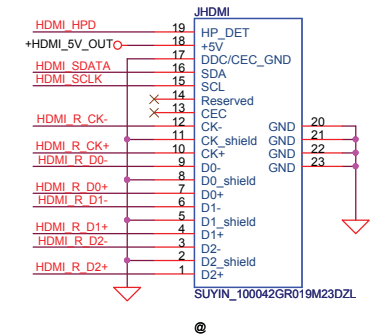
## CRT CONNECTOR



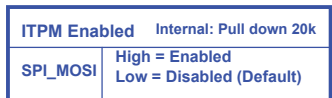
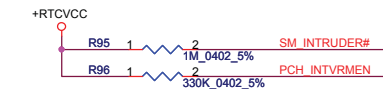
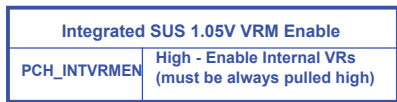
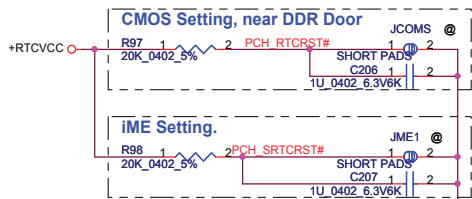
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		PBL01 LA6733P M/B		0.3		
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## HDMI Connector

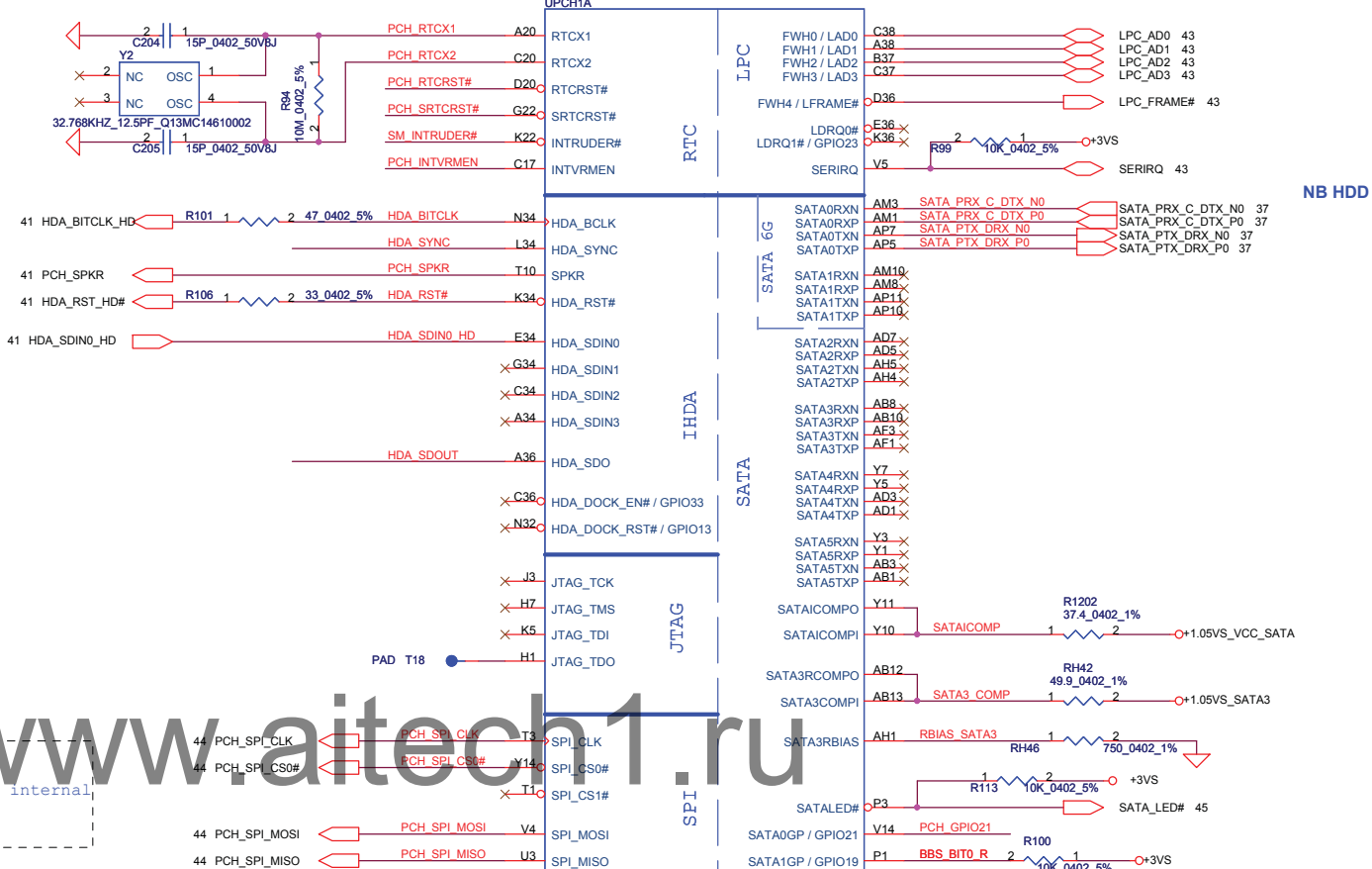
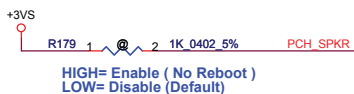
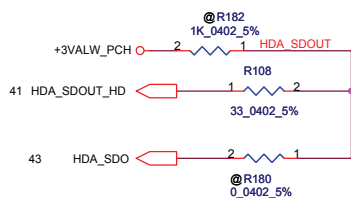
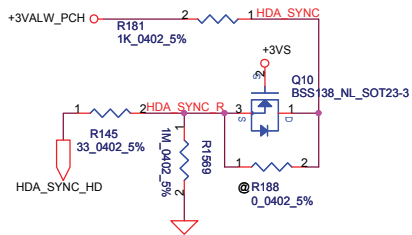


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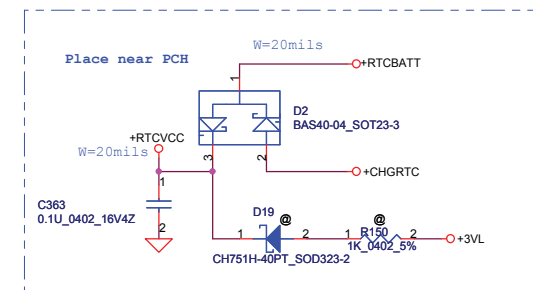


**HDA\_SYNC**  
This signal has a weak internal pull down.  
H=>On Die PLL is supplied by 1.5V  
L=>On Die PLL is supplied by 1.8V

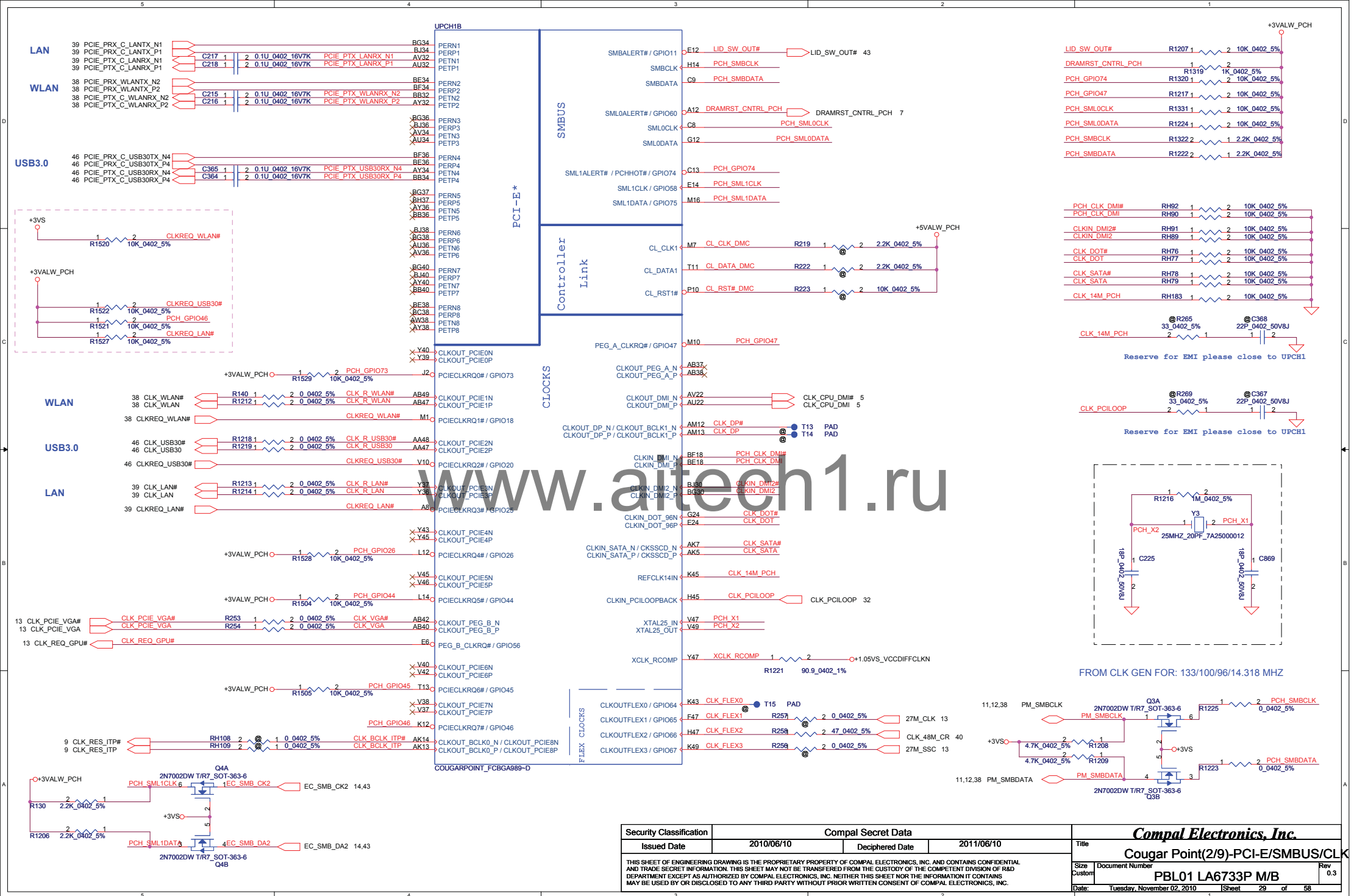
**HDA\_SDO**  
This signal has a weak internal pull down.  
This signal can't PU



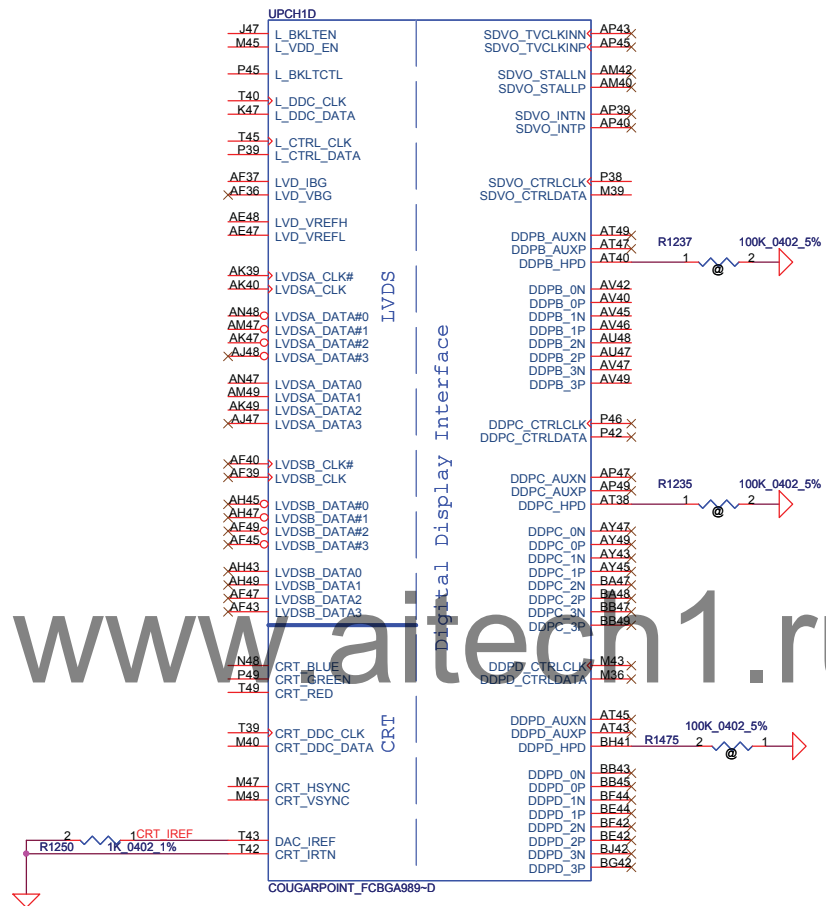
Project ID	GPIO21
★ 13"	0
14"	1



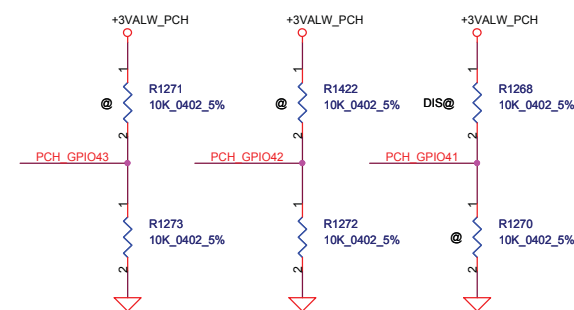
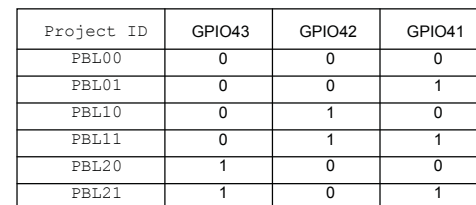
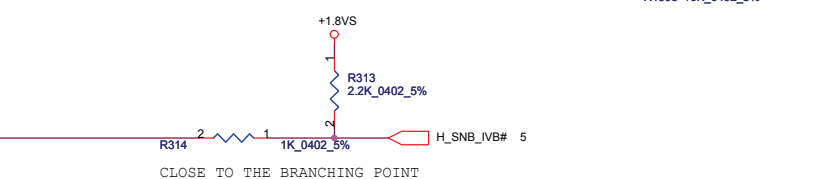
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								Cougar Point(1/9)-HDA/SATA/XDP/RTC/SP	
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						Custom	PBL01 LA6733P M/B		0.3
						Date	Tuesday, November 02, 2010		Sheet
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			58						



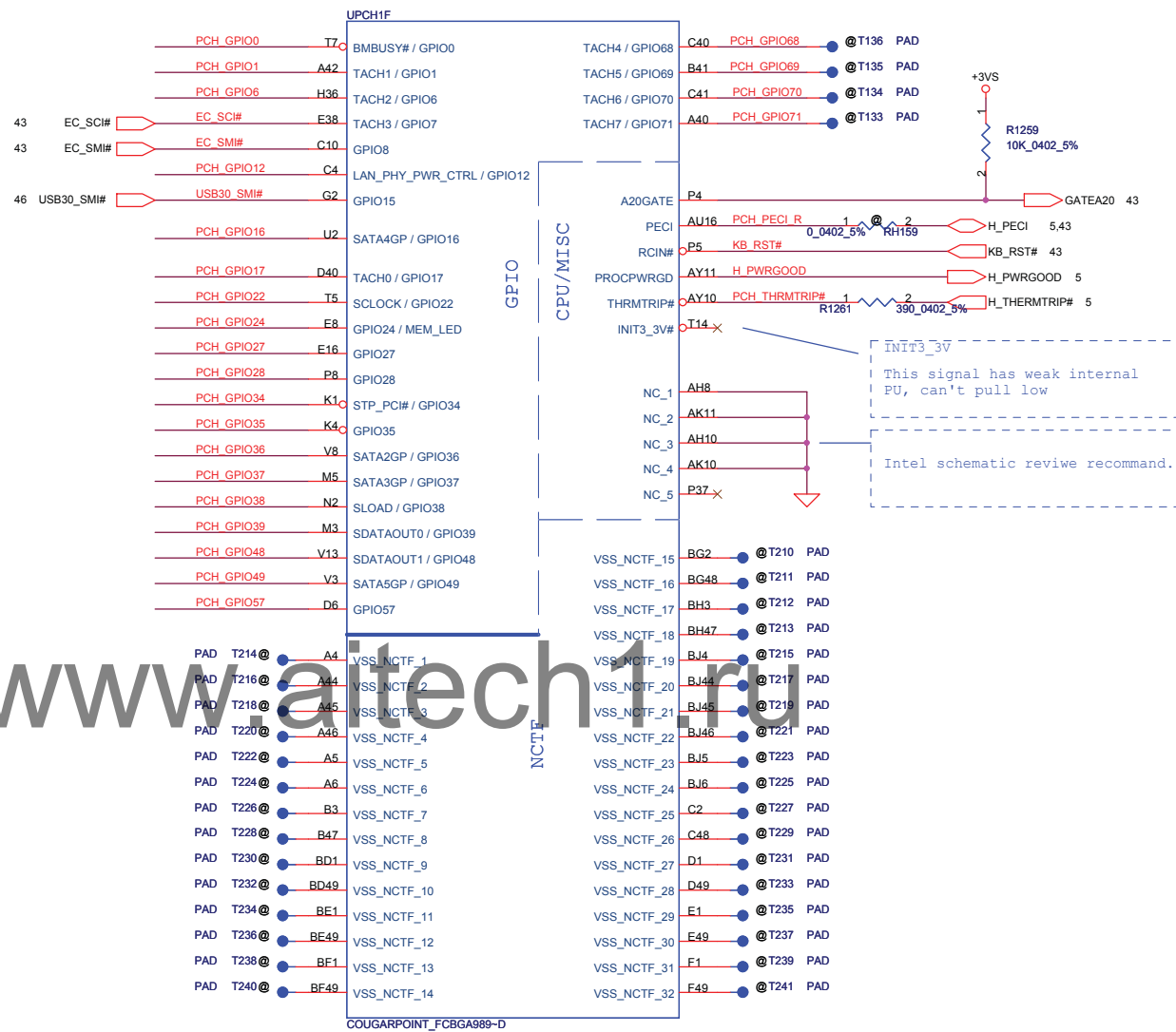
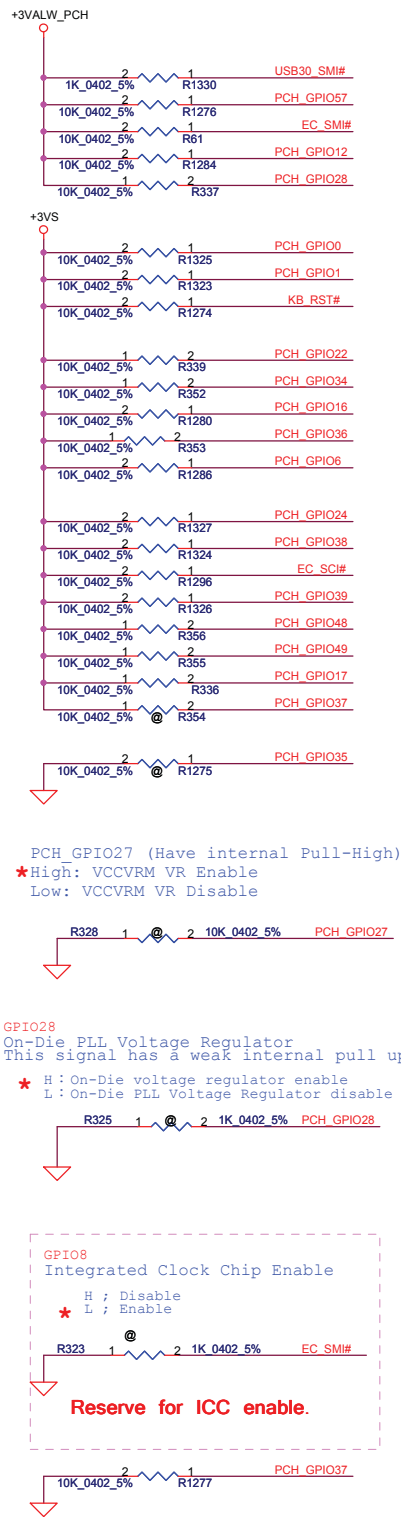




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Issued Date	2010/06/10	Deciphered Date	2011/06/10	Title	Cougar Point(4/9)-CRT/LVDS/HDMI/DP
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				Date	Monday, October 25, 2010
				Sheet	31 of 58
				Rev	0.3

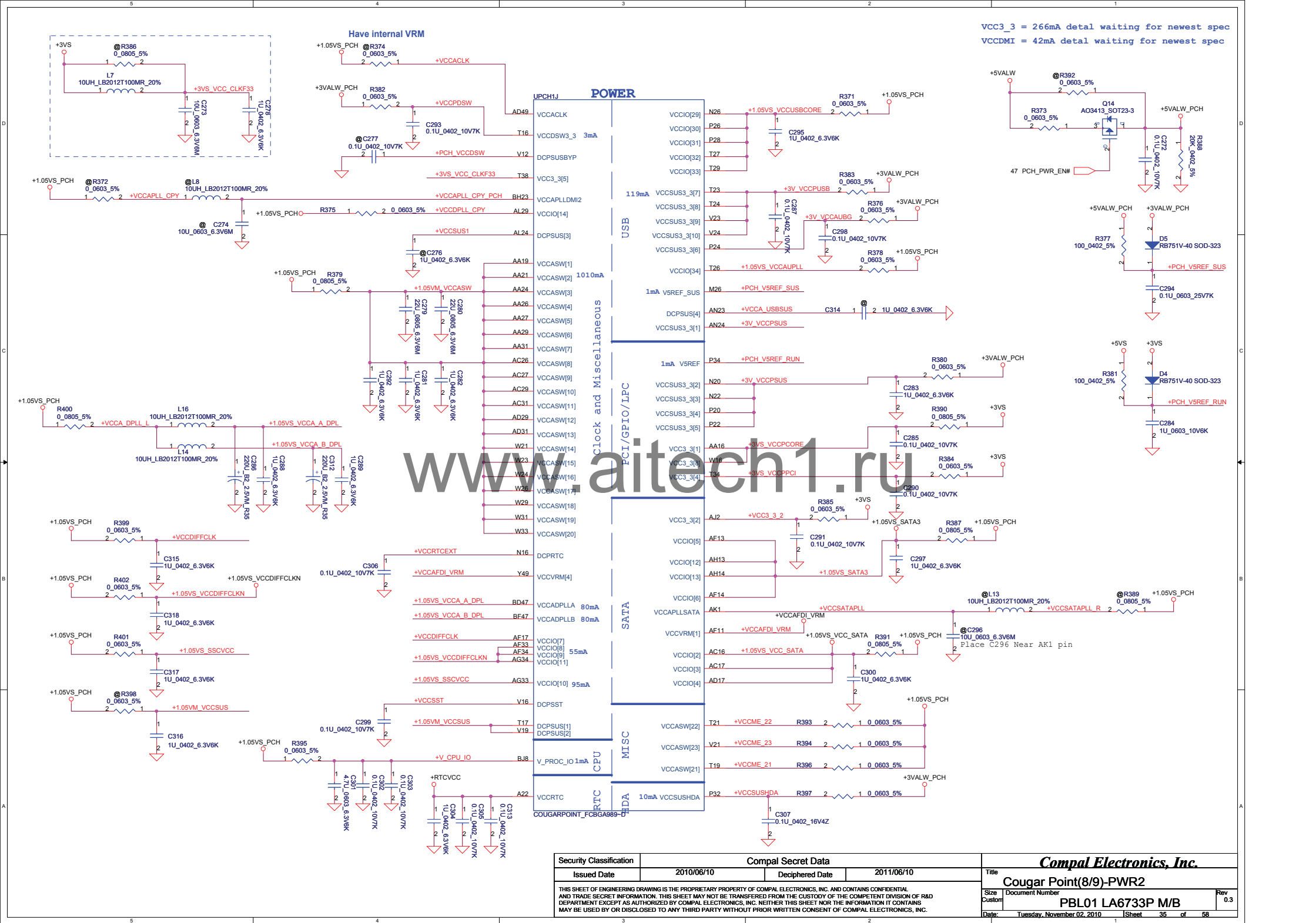


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				Custom	PBL01 LA6733P M/B	0.3
				Date:	Tuesday, November 02, 2010	Sheet 32 of 58

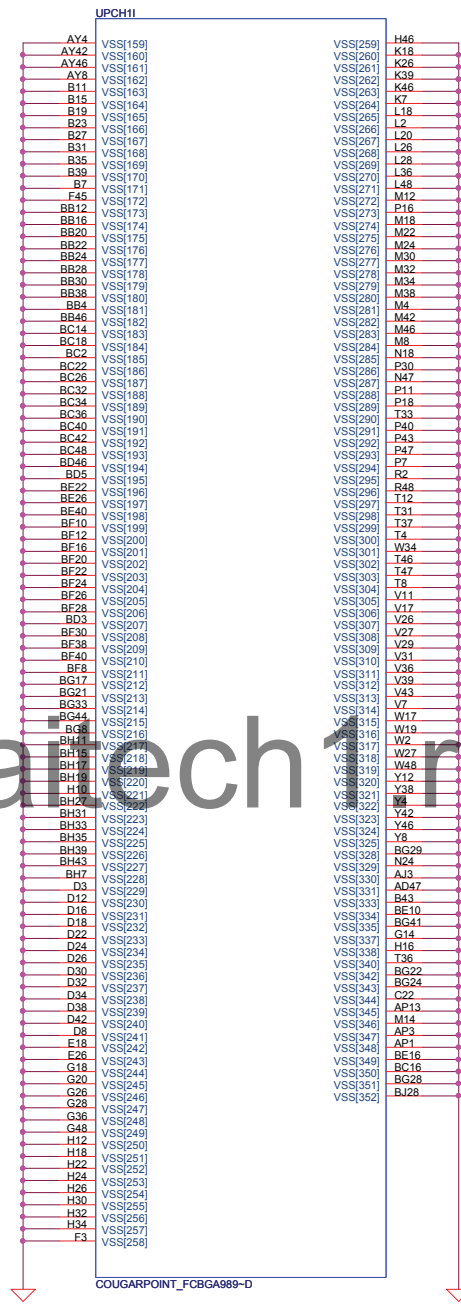
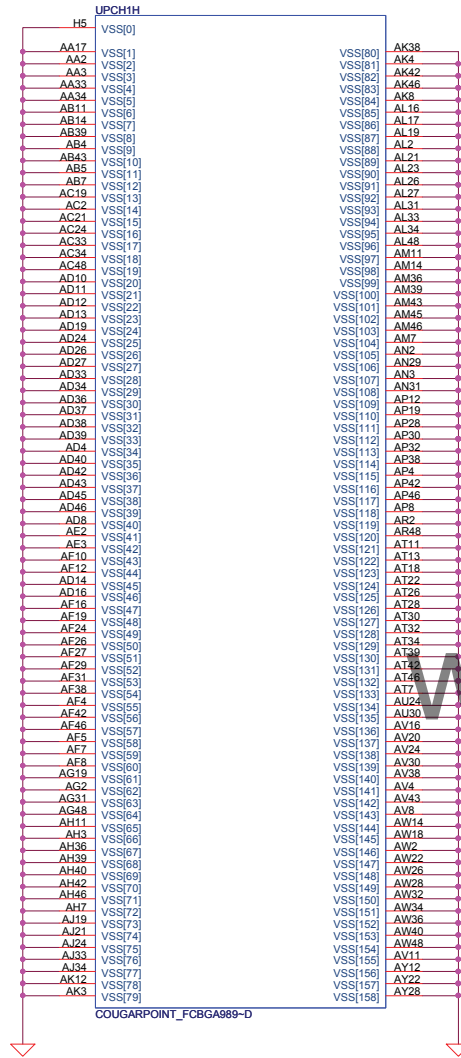


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Issued Date	2010/06/10	Deciphered Date	2011/06/10	Title	Cougar Point(6/9)-CPU/GPIO/MISC
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				Date	Tuesday, November 02, 2010
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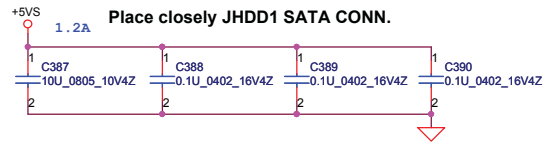


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				Custom	PBL01 LA6733P M/B	0.3
				Date:	Tuesday, November 02, 2010	Sheet 35 of 58

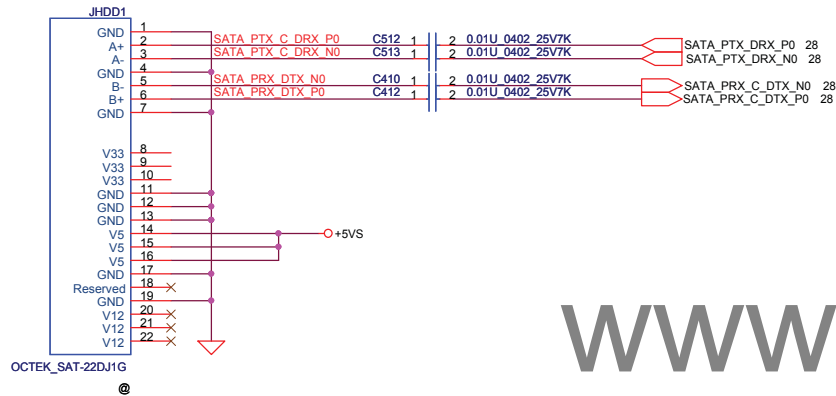


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				Date Monday, October 25, 2010	Rev 0.3
				Sheet 36	of 58

## SATA HDD1 Conn.



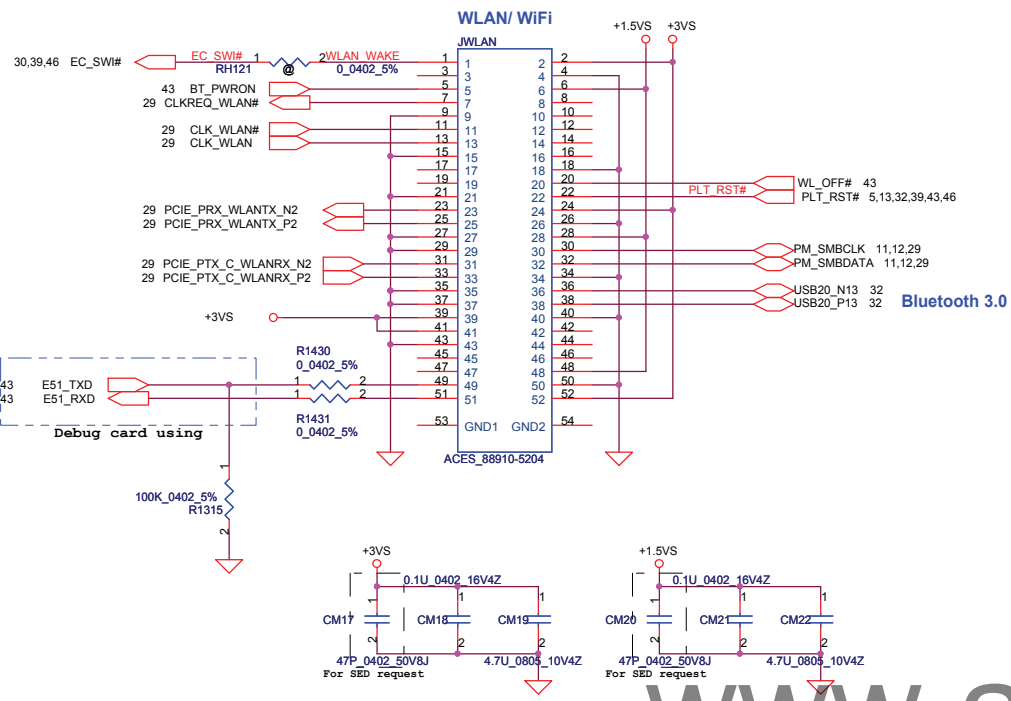
## 13.3" HDD



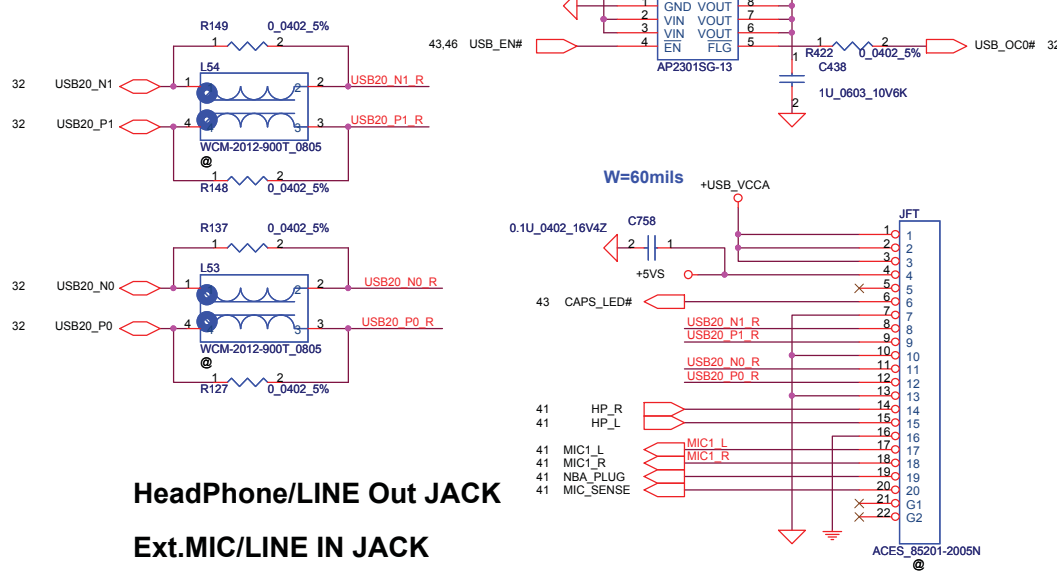
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Slot 1 Half PCIe Mini Card-WLAN & BT3.0



Function Board



HeadPhone/LINE Out JACK  
Ext.MIC/LINE IN JACK

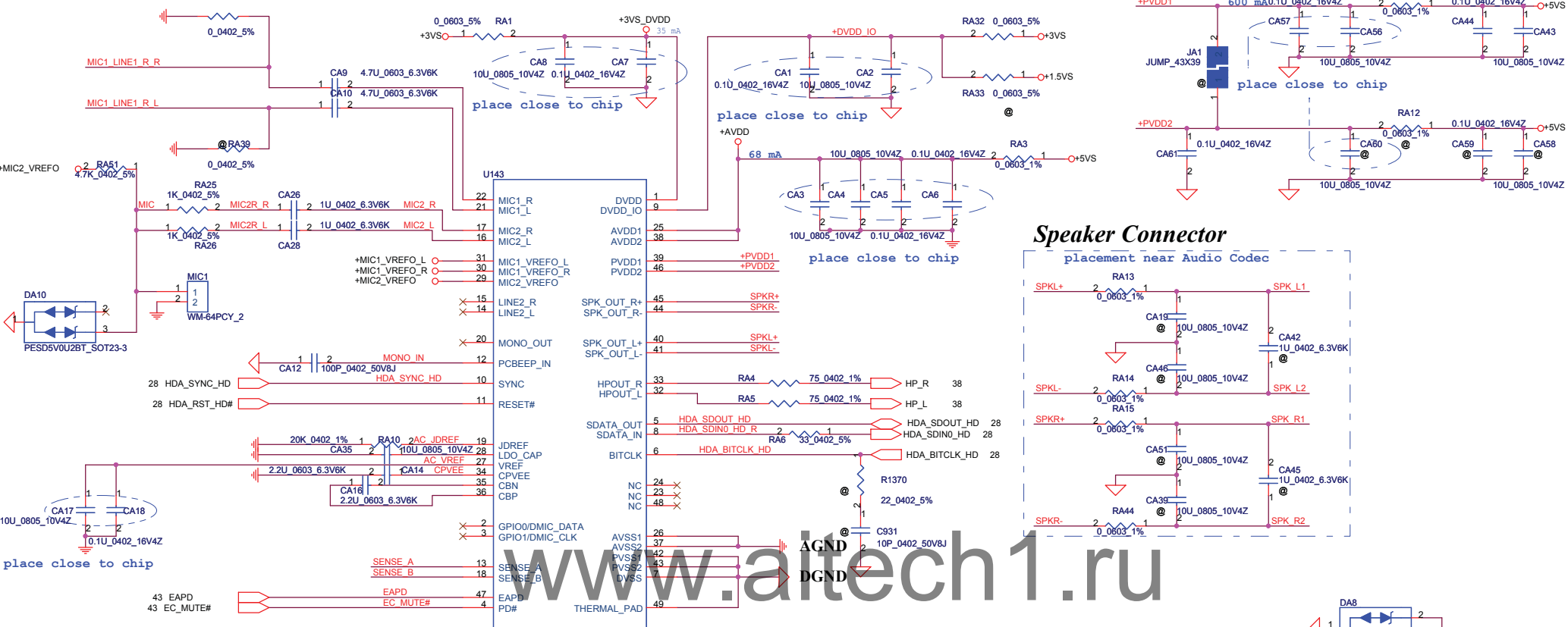
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				Date	Tuesday, November 02, 2010
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				Rev	0.3

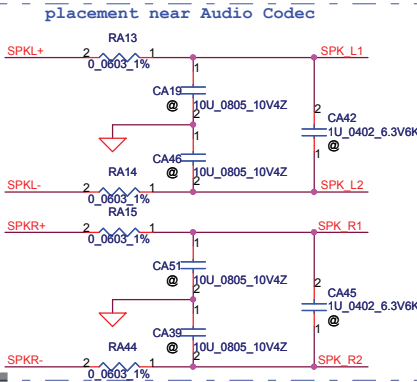




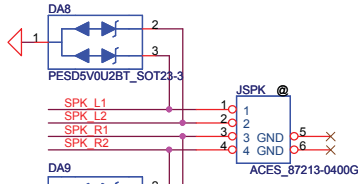
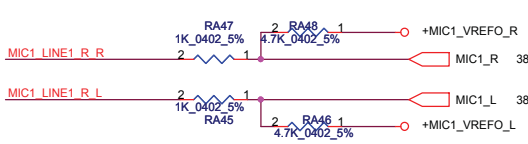
Ext. Mic/LINE IN



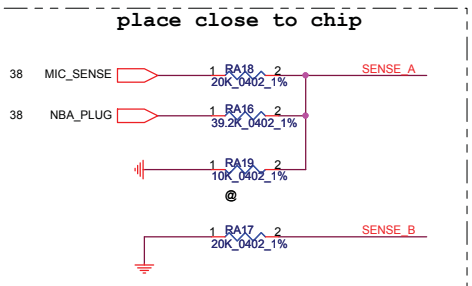
Speaker Connector



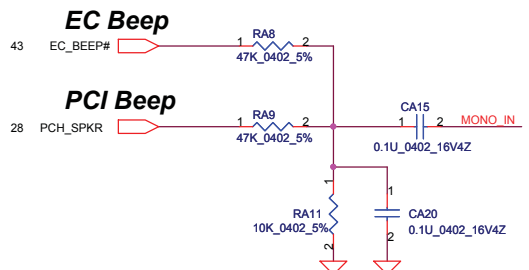
Ext. MIC/LINE IN JACK



Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	SPK out
	5.1K	PORT-D (PIN 35, 36)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	Int. MIC
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 37)	
	5.1K	PORT-I (PIN 32, 33)	



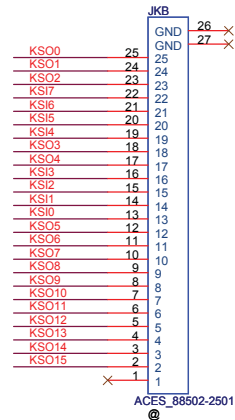
Beep sound



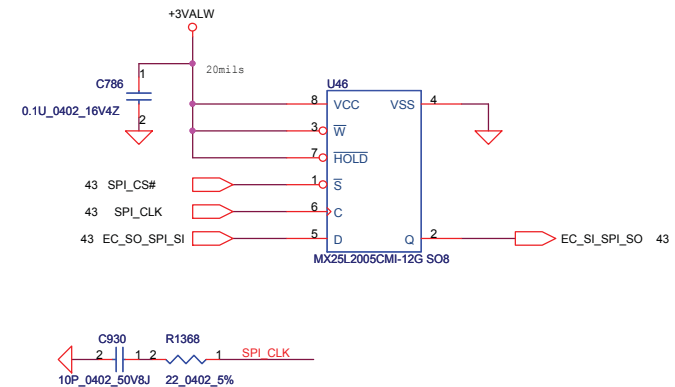
## KEYBOARD CONN.

For EMC

KSO10	1	2
C803	100P_0402_50V8J	
KSO11	1	2
C804	100P_0402_50V8J	
KSO12	1	2
C805	100P_0402_50V8J	
KSO15	1	2
C807	100P_0402_50V8J	
KSI7	1	2
C808	100P_0402_50V8J	
KSI2	1	2
C810	100P_0402_50V8J	
KSI3	1	2
C811	100P_0402_50V8J	
KSI4	1	2
C812	100P_0402_50V8J	
KSI5	1	2
C813	100P_0402_50V8J	
KSI6	1	2
C814	100P_0402_50V8J	
KSI1	1	2
C815	100P_0402_50V8J	
KSI1	1	2
C816	100P_0402_50V8J	
KSO2	1	2
C793	100P_0402_50V8J	
KSO1	1	2
C790	100P_0402_50V8J	
KSO4	1	2
C791	100P_0402_50V8J	
KSO3	1	2
C792	100P_0402_50V8J	
KSO5	1	2
C795	100P_0402_50V8J	
KSO14	1	2
C796	100P_0402_50V8J	
KSO6	1	2
C797	100P_0402_50V8J	
KSO7	1	2
C798	100P_0402_50V8J	
KSO13	1	2
C799	100P_0402_50V8J	
KSO8	1	2
C800	100P_0402_50V8J	
KSO9	1	2
C801	100P_0402_50V8J	
C802	100P_0402_50V8J	



## SPI Flash (1MByte\*1)

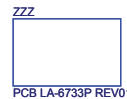


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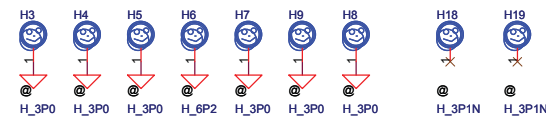
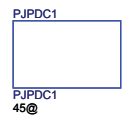
Screw Hole

ISPD

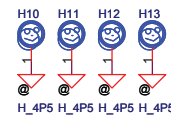
PCB



DC-IN



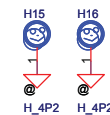
CPU



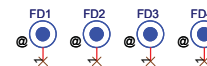
JWLAN



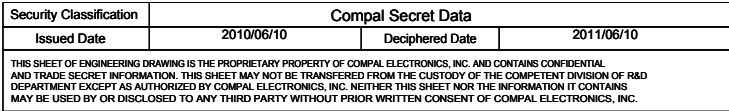
VGA



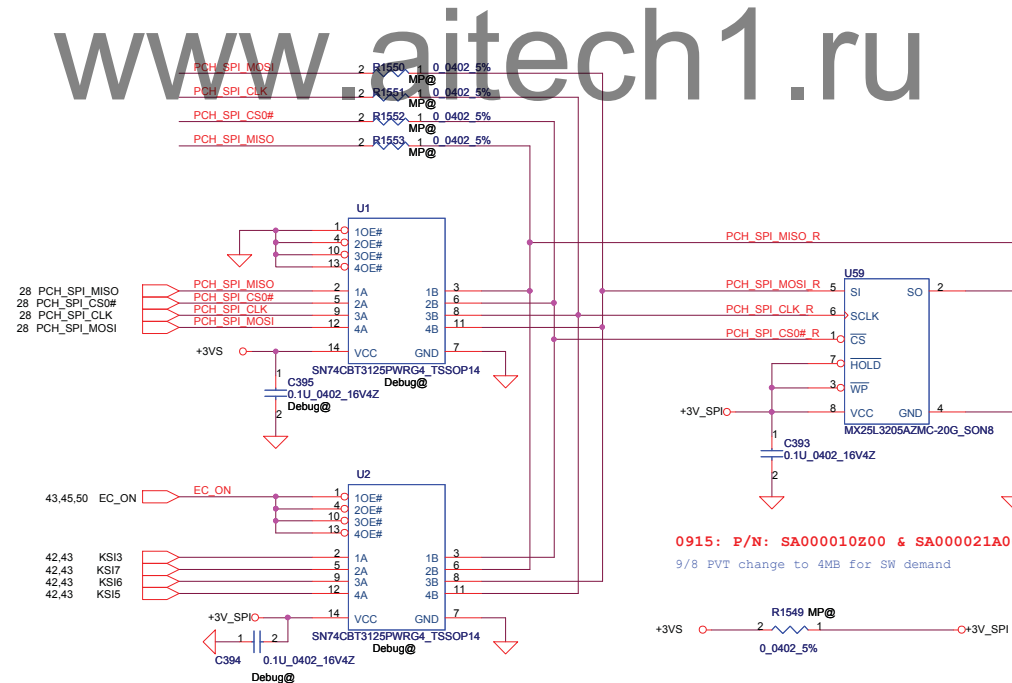
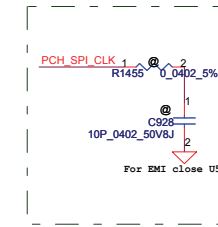
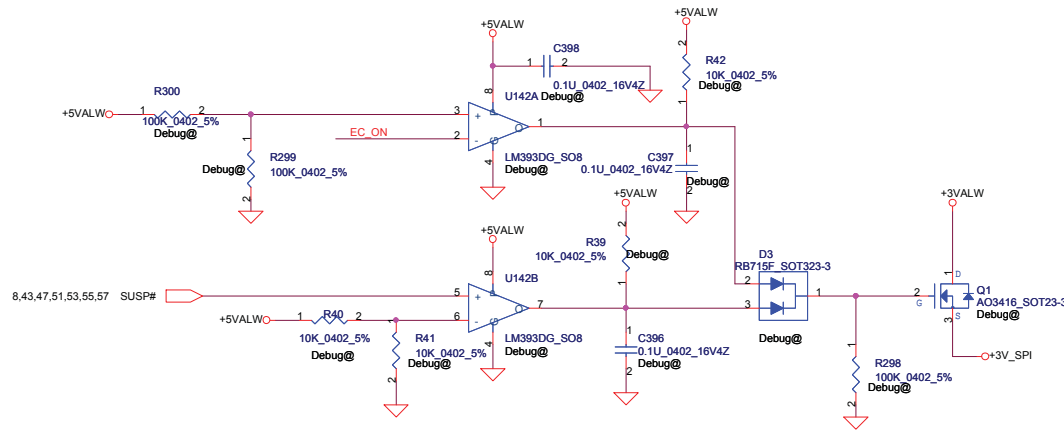
PCB Federal Mark PAD



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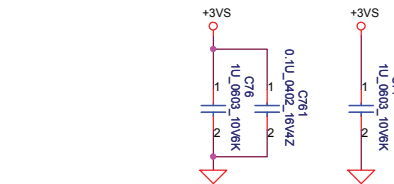
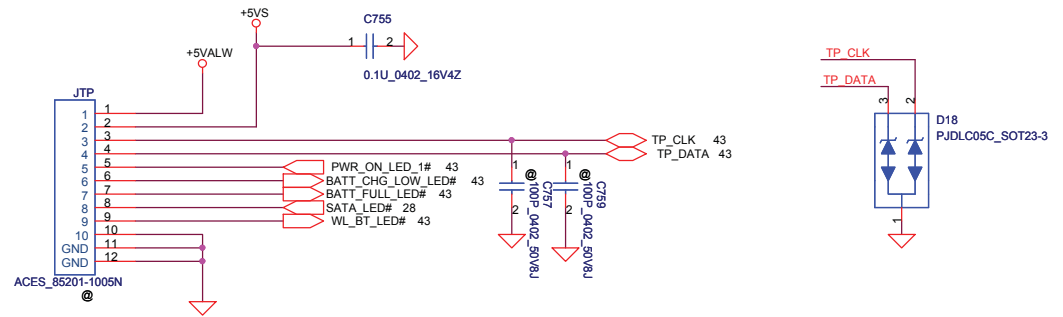


**SPI ROM For Basic ME ROM size  
(w/o Braidwood & system BIOS):  
4MByte**



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Size		Document Number		Rev	
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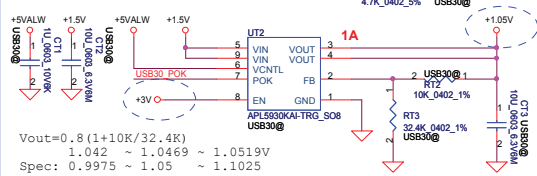
## Touch/B Connector



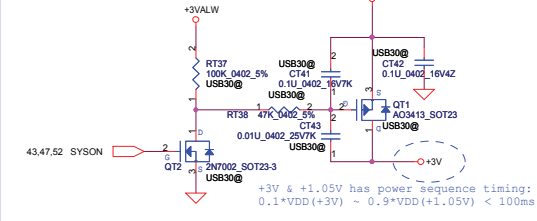
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				PBL01 LA6733P M/B			0.3
				Date:	Tuesday, November 02, 2010	Sheet	45 of 58

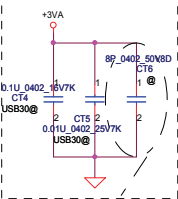
## +1.5V to +1.05V Transfer



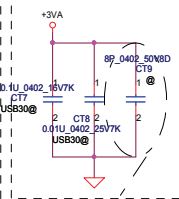
## +3VALW to +3V Transfer



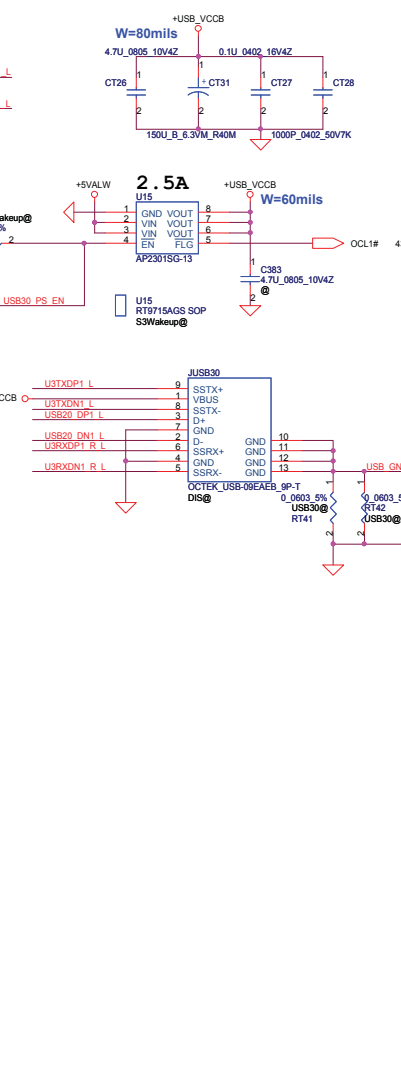
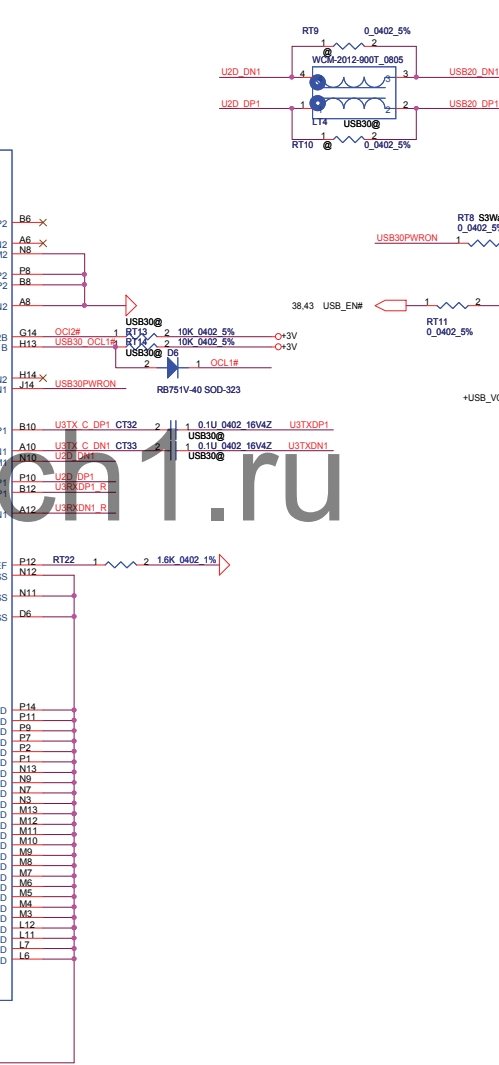
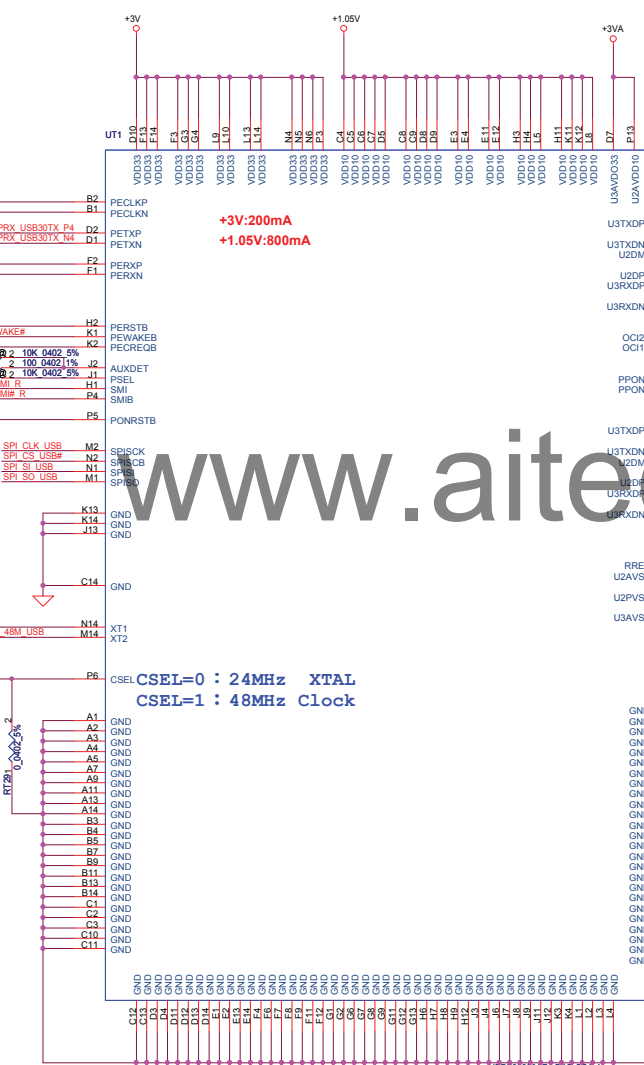
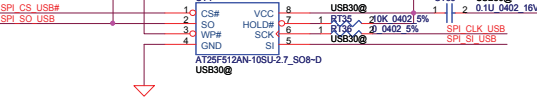
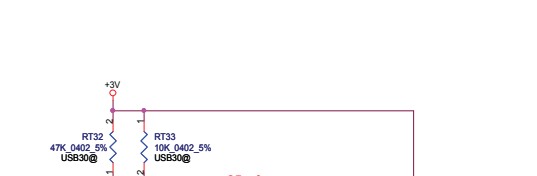
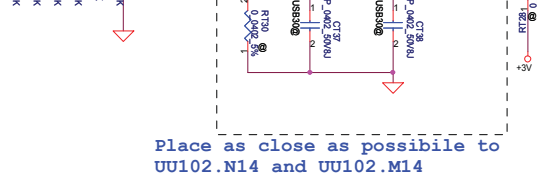
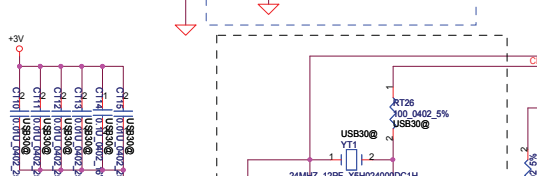
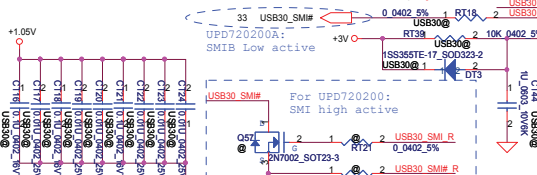
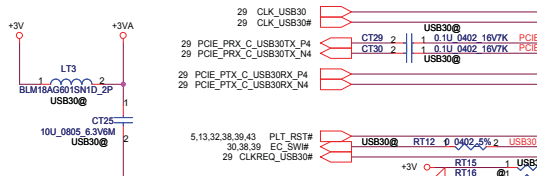
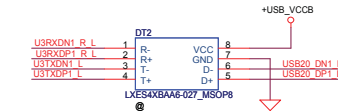
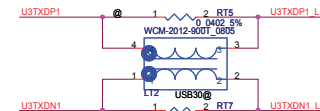
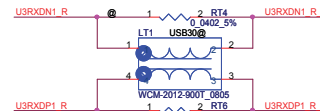
### Close to U102.D7



### Close to U102.P13



Follow Vendor recommend.



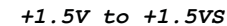
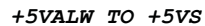
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Place as close as possible to U102.N14 and U102.M14

SPI CLK USB RT34 2 0.1U 0402 16V7K

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0.3					

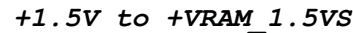
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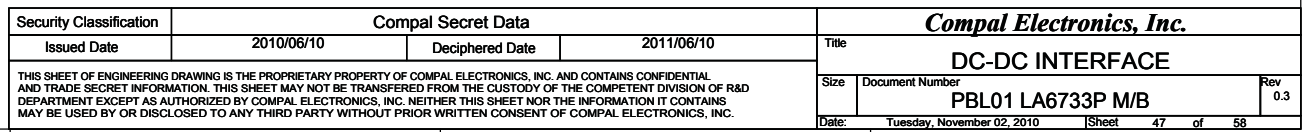
$V_{gs}=10V, I_d=14.5A, R_{ds}=6m\Omega$



$V_{gs} = -4.5V, I_d = 3A, R_{ds} < 97m\Omega$

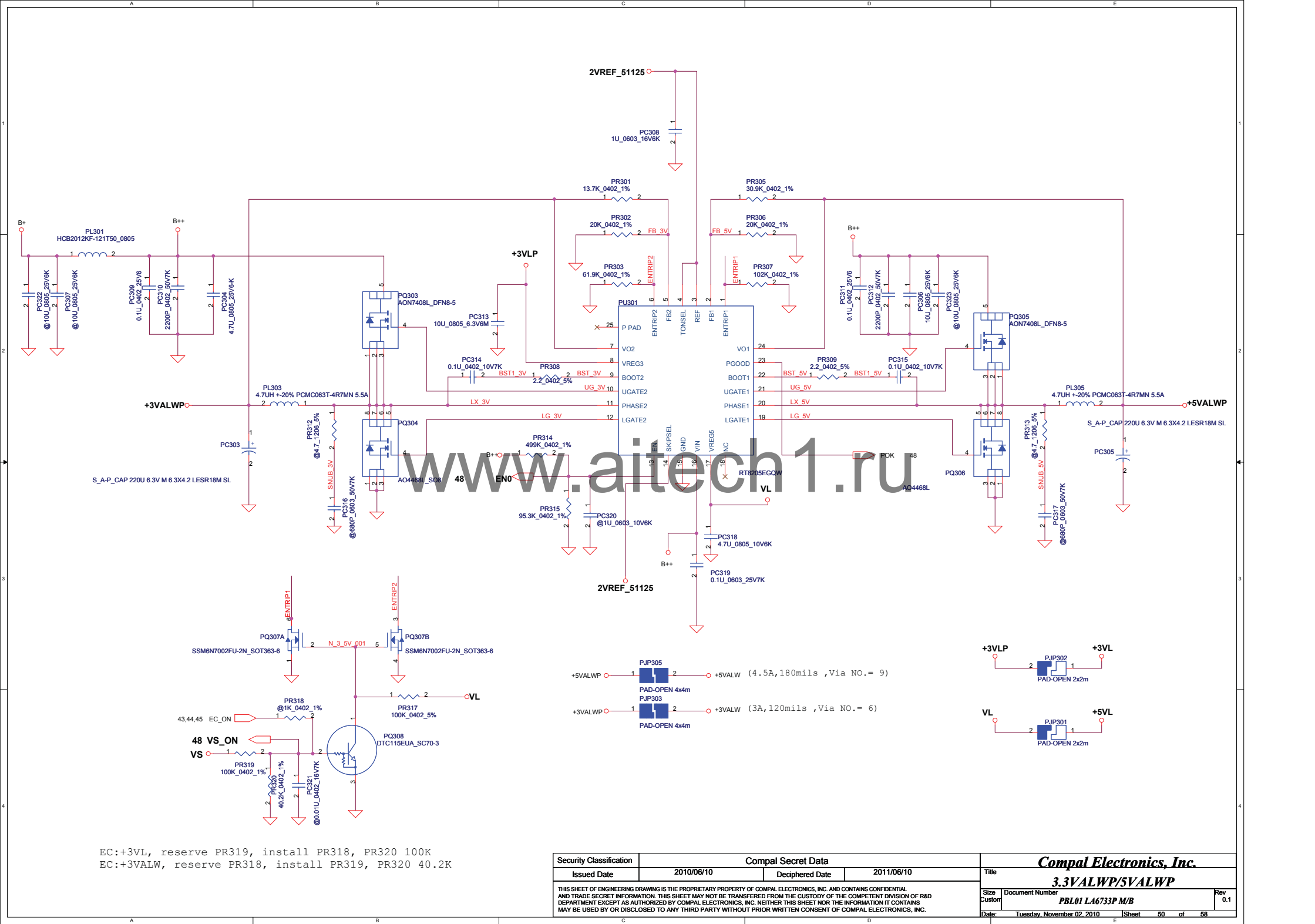


Short J1 for PCH VCCSUS3.3



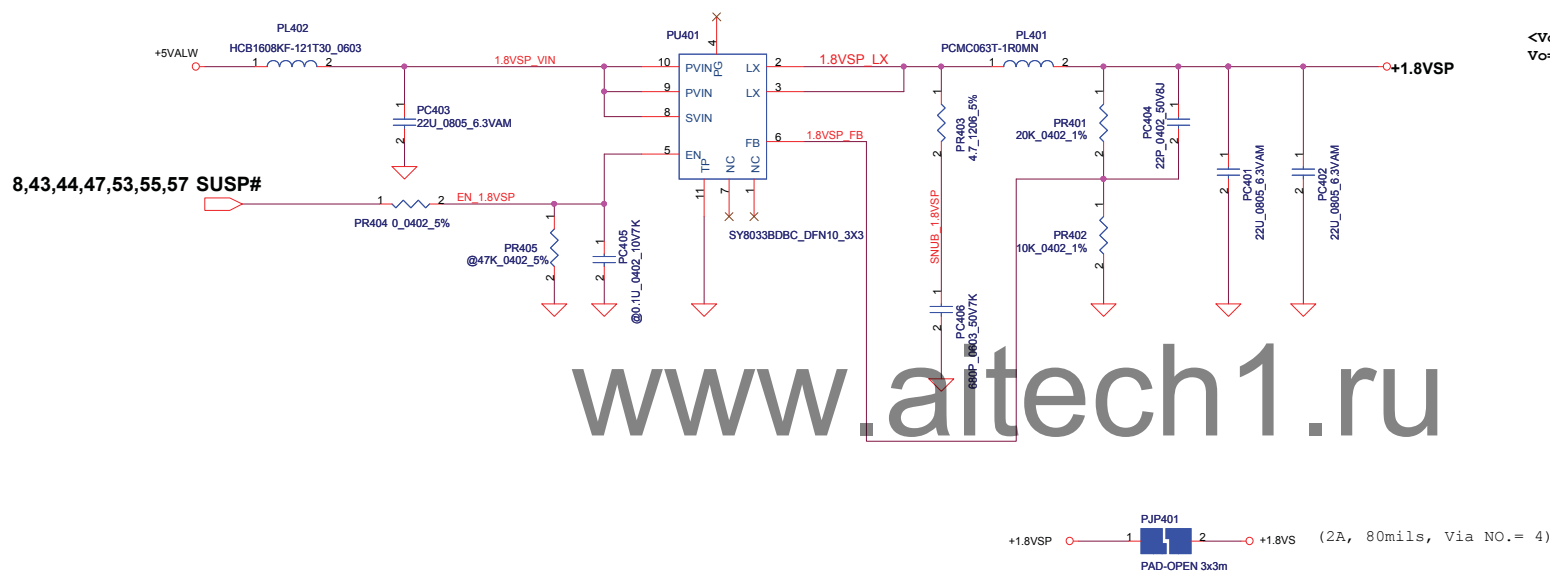






EC:+3VL, reserve PR319, install PR318, PR320 100K  
 EC:+3VALW, reserve PR318, install PR319, PR320 40.2K

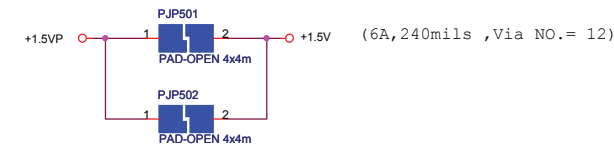
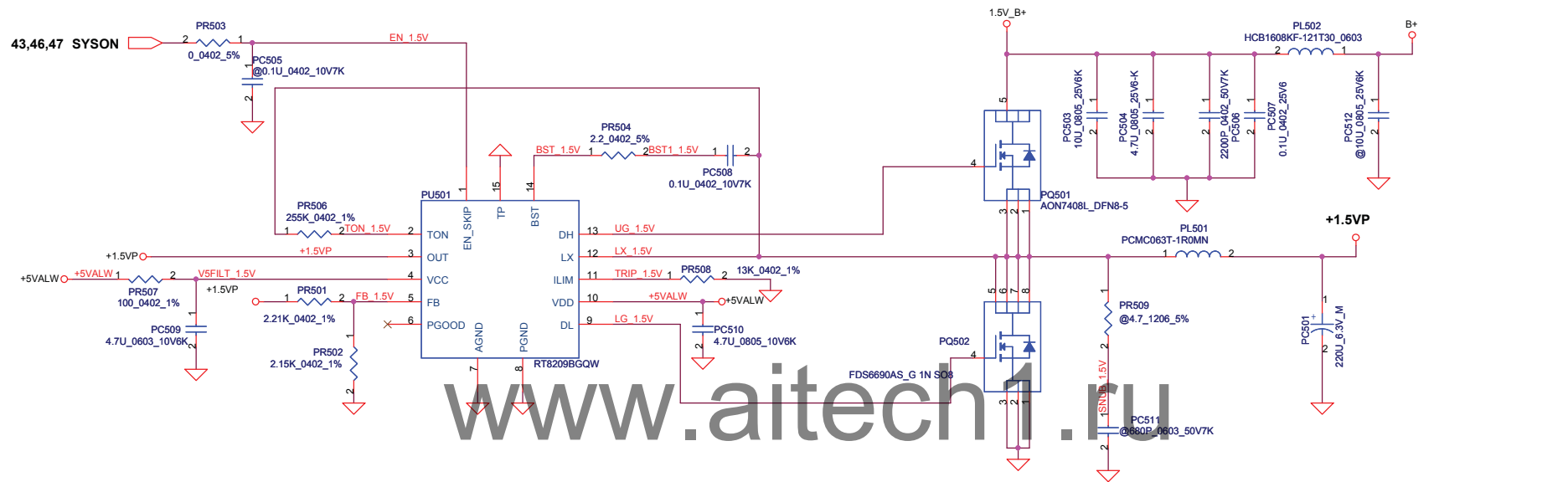
Security Classification		Compal Secret Data		Title	
Issued Date	2010/06/10	Deciphered Date	2011/06/10	3.3VALWP/5VALWP	
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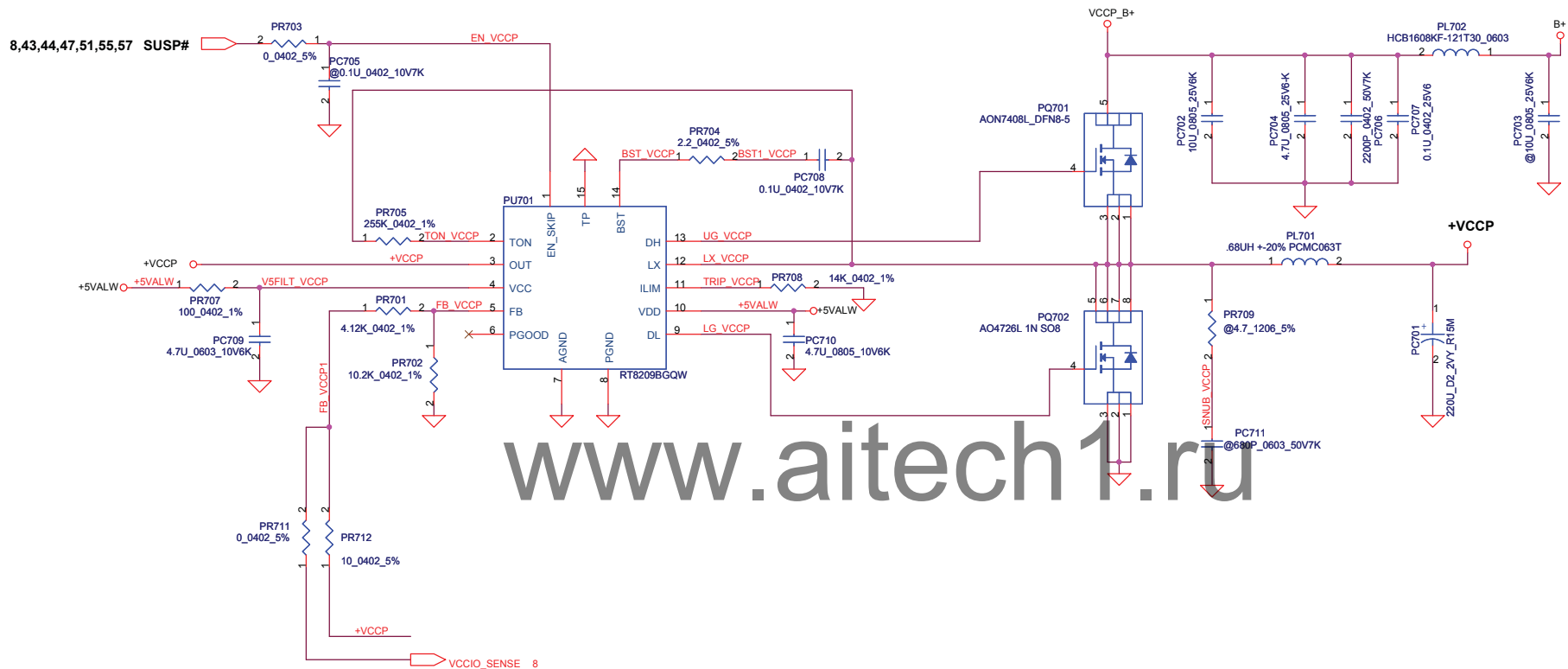
$$\langle V_o = 1.8V \rangle \quad V_{FB} = 0.6V$$

$$V_o = V_{FB} * (1 + PR401 / PR402) = 0.6 * (1 + 20K / 10K) = 1.8V$$

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VSSIO\_SENSE connect to GND directly.

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					<b>PBL01 LA6733P M/B</b>	0.1
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Revision Change: 0.1 to 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	08/12	All	Remove all components about UMA@	From UMA/DIS schematic to DIS only
2	08/12	41	Change RA16 from 5.1K to 39.2K & connect from SENSE_B to SENSE_A	Headphone out can't detect issue
3	08/12	46	Change USB30 from TI to NEC	SPEC request
4	08/12	27	Delet U37 and relate schematic. Q16.1 connect to HDMI connector directly. R570 from 100K to 20K	HDMI Hot Plug issue
5	08/24	41	Change RA9,RA10 to 4.7U	For Audio Precision
6	08/24	29	Change CLKREQ_USB30# Pull-hi from +3VS to +3VALW_FCH	Vendor request
7	08/25	43	Mount R1368 and C930	EMI request
8	08/25	28,29,32	Change R101,R258, and R1545 to 47ohm	EMI request
9	08/25	5	Add R15 between PLT_RST# to U3	EMI request
10	08/25	25	Change C399 to 1U_0603	EMI request
11	08/25	45	Add C760	EMI request
12	08/26	10	Remove C80	DFB issue
13	08/26	45	Change CT31 footprint to B2	DFB issue
14	08/31	45	Add C73,C76,C77, and C761	EMI issue
15	09/01	14	Remove RV33,RV34	ME issue
16	09/02	41	Reserve C931 and R1370	EMI request
17	09/02	43	Remove C208	EMI request

Revision Change: 0.2 to 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	10/08	28	Add R1569	Power consumption
2	10/20	43	Add R725 and pull high +3VALW	For common design
3	10/20	46	Remove DT1	For cost down
4	10/20	27	Remove D17	For cost down
5	10/22	39	Reserve D22, D23	EMI request
6	10/27	43	Add R726 and pull high +3VALW	For common design
7	10/28	43	Add R138 and pull low to GND	EC request

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